erating a stop signal when the level of cells in the respective output buffer reaches a second threshold.

3. The ATM switch of claim 1, further comprising:

connection admission control for issuing queue timestamps for each cell in said plurality of input buffers;

a timer issuing a current time; and,

wherein said input module scheduler further comprises a comparator for comparing said queue timestamps to said current time, and scheduling eligibility for service each of said cells having queue timestamp equal to current time.

4. The ATM switch of claim 3, wherein each of said input module scheduler and output module scheduler further comprises:

a timestamp storage unit for storing the queue timestamps and providing said queue timestamps to said comparator;

a virtual rate shaping unit connected to said comparator for shaping transmission rate of cells eligible for service;

a plurality of virtual queue counters for counting the number of cells eligible for service;

a service scheduling unit for scheduling cells eligible for service;

a compute engine for dynamically updating the timestamps.

5. The ATM switch of claim 4, further comprising a rate feedback from said output modules to said input modules.

6. The ATM switch of claim 1, wherein said plurality of output buffers of said core switch are designated real-time output buffers and wherein said core switch further comprises:

a plurality of non-real-time output buffers corresponding to the number of real-time output buffers and each connected to one of said output ports;

a non-real-time multicast buffer connected to each of said output ports.

7. An ATM switch capable of supporting cell streams of different classes having various quality of service requirements, comprising:

a core switch comprising:

a TDM bus;

a plurality of input ports connected to said TDM bus;

a plurality of output buffers connected to said TDM bus;

a plurality of output ports connected to respective output buffers; and

a multicast output buffer connected to each of said output ports;

a plurality of output modules connected to output side of said core switch, each of said output modules having a plurality of output lines and comprising:

a plurality of output line planes, each having a plurality of output line buffers coupled to said output lines;

an output module scheduler for scheduling cells in said output buffers;

a plurality of input modules connected to input side of said core switch, each of said input modules comprising:

a plurality of output port planes corresponding to the number of said output ports, each of said output port planes having a plurality of output line planes corresponding to the number of said output lines, each of said output line planes having a plurality of input buffers;

an input module scheduler for scheduling cells in said input buffers.

8. The ATM switch of claim 7, wherein each of said output buffers of said core switch comprises overflow control for generating a shape signal when level of cells in a respective output buffer reaches a first threshold, and generating a stop signal when the level of cells in the respective output buffer reaches a second threshold.

9. The ATM switch of claim 7, further comprising:

connection admission control for issuing queue timestamps for each cell in said plurality of input buffers;

a timer issuing a current time; and,

wherein said input module scheduler further comprises a comparator for comparing said queue timestamps to said current time, and scheduling eligibility for service each of said cells having queue timestamp equal to current time.

10. The ATM switch of claim 9, wherein each of said input module scheduler and output module scheduler further comprises:

a timestamp storage unit for storing the queue timestamps and providing said queue timestamps to said comparator;

a virtual rate shaping unit connected to said comparator for shaping transmission rate of cells eligible for service;

a plurality of virtual queue counters for counting the number of cells eligible for service;

a service scheduling unit for scheduling cells eligible for service;

a compute engine for dynamically updating the timestamps.

11. The ATM switch of claim 10, further comprising a rate feedback from said output modules to said input modules.

12. The ATM switch of claim 7, wherein said plurality of output buffers of said core switch are designated real-time output buffers and wherein said core switch further comprises:

a plurality of non-real-time output buffers corresponding to the number of real-time output buffers and each connected to one of said output ports;

a non-real-time multicast buffer connected to each of said output ports.

13. An ATM switch capable of supporting streams of different classes having various quality of service requirements, comprising:

a core switch comprising:

a TDM bus;

a plurality of input ports connected to said TDM bus;

a plurality of output buffers connected to said TDM bus;

a plurality of output ports connected to respective output buffers;

a plurality of input modules connected to input side of said core switch, each of said input modules comprising:

a plurality of input buffers;

a connection admission control assigning a minimum guaranteed rate and an excess share weight for each of said input buffers;

an input module scheduler for scheduling cells in said input buffers according to a rate composed of said minimum guaranteed rate and a share of the available unused bandwidth, said share being proportional to the excess share weight.

14 The ATM switch of claim 13, further comprising a closed-loop controller for adjusting the available unused bandwidth according to cell occupancy of said output buffers.

15 The ATM switch of claim 14, further comprising an overload control for transmitting a shape rate signal from any of said output buffers whenever cell occupancy of a respective one of said output buffers reaches a predetermined shape threshold, and wherein said scheduler is responsive to said shape signal to schedule said input buffers according to the guaranteed minimum rate only

16 A tripled buffered ATM switch capable of supporting streams of different classes having various quality of service requirements, comprising:

a plurality of input buffers for queuing incoming cell streams;

a plurality of core buffers receiving queued cells of said cell streams from said input buffers and providing said queued cell to respective output ports;

a plurality of output buffers receiving said queued cells from said output ports and providing said queued cell to respective output lines;

a scheduler for scheduling transmission of said queued cells from said input buffers;

a first feedback loop from said core buffers to said scheduler, for transmission of load information of said core buffers to said scheduler;

a second feedback loop from said output buffers to said scheduler, for transmission of load information of said output buffers to said scheduler;

wherein said scheduler schedules transmission of said queued cells from said input module according to information received from said first and second feedback loops.

17 The tripled buffered ATM switch according to claim 16, further comprising a connection admission control for assigning a minimum guaranteed rate to said cell streams, and wherein said scheduler schedules said queued cells at the input buffers at a rate not less than said minimum guaranteed rate.

18 The tripled buffered ATM switch according to claim 17, wherein said scheduler schedules said queueds at the input buffers according to a dynamic rate which comprises the minimum guaranteed rate plus a distribution of an unused bandwidth determined from the information of said first and second feedback loops.

19 The tripled buffered ATM switch according to claim 18, wherein said connection admission control further assigns queue timestamps to each of said queues, and wherein said scheduler further comprises a comparator for comparing the queue timestamps to current time and defining each queue having a queue timestamp equal to or less than the current time as eligible for service

20 A scheduler for an ATM switch, comprising:

a first memory for storing cells timestamps assigned to cells in queues to be scheduled;

a second memory for storing actual queue load;

a third memory for storing cells in virtual queues;

a current time generator generating current time;

a plurality of comparators for comparing the cells timestamps to current time and designating cells having cell timestamps≧current time as eligible for service;

a virtual rate selector for assigning cells from said eligible cells to said virtual queues;

a service scheduling selector which selects queues for service from said virtual queues;

a compute engine for scheduling and rescheduling cells in said first memory.

21 A buffer, comprising:

a first monitoring circuit for monitoring a load level in said buffer and for generating a shape signal when said load level reaches a first threshold, so as to cause input to said buffer to be reduced to a minimum level, and further for generating a stop signal when said load level reaches a second threshold, so as to halt any input to said buffer

22 The buffer of claim 21, further comprising an estimation circuit for estimating an unused bandwidth available on said buffer and generating a signal indicating said estimated bandwidth.

23 A scheduler for an ATM switch, comprising:

a first memory for storing queue timestamps assigned to queues to be scheduled;

a second memory for storing actual queue load;

a third memory for storing cells in virtual queues;

a current time generator generating current time;

a plurality of comparators for comparing the queue timestamps to current time and designating queues having cell timestamps≦current timestamp as eligible for service;

a virtual rate selector for assigning cells from said eligible cells to said virtual queues;

a service scheduling selector which selects queues for service from said virtual queues;

a compute engine for scheduling and rescheduling cells in said first memory.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,324,165 B1
DATED : November 27, 2001
INVENTOR(S) : Ruixue Fan, Brian L. Mark, Gopalakrishnan Ramamurthy

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 1,
Line 5, delete "08/929,820" insert -- 08/924,820 --

Column 11,
Line 33, delete "$R_{i=}M_{i+wi}E$" insert -- $R_{i=}M_{i+wi}E$ --

Column 16,
Line 14, delete "WF_j" insert -- WF_{ij} --

Column 21,
Line 7, delete "U_2" insert -- U_0 --

Column 30,
Line 13, delete "≧" insert -- ≤ --

Signed and Sealed this

Twenty-sixth Day of March, 2002

Attest

Attesting Officer

JAMES E. ROGAN
Director of the United States Patent and Trademark Office

US005315586A

United States Patent [19]

Charvillat

[11] Patent Number: 5,315,586

[45] Date of Patent: May 24, 1994

[54] RESOURCE REALLOCATION FOR FLOW-ENFORCED USER TRAFFIC

[75] Inventor: Eric Charvillat, Tokyo, Japan

[73] Assignee: NEC Corporation, Japan

[21] Appl. No.: 905,794

[22] Filed: Jun. 29, 1992

[30] Foreign Application Priority Data

Jun. 28, 1991 [JP] Japan 3-157240

[51] Int. Cl.[5] H04J 3/26

[52] U.S. Cl. 370/60; 370/61; 370/94.1

[58] Field of Search 370/17, 60, 60.1, 61, 370/79, 84, 85.6, 85.7, 94.1, 94.2, 94.3, 95.1, 110.1, 118

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Primary Examiner—Douglas W. Olms
Assistant Examiner—Melvin Marcelo
Attorney, Agent, or Firm—Ostrolenk, Faber, Gerb & Soffen

[57] ABSTRACT

In a packet (ATM) network, a source node at the entry of the network is responsive to a connection request from a user terminal for invoking a CAC (call admission control) algorithm to accept or reject the request depending on the amount of resource requested by the user, and allocates a portion of a free bandwidth resource exclusively to the user for the duration of the call according to established contract parameter values. Each node of the network responds to a reallocation request from the user for transmitting a copy of the request to a downstream node to elicit an acceptance message therefrom, and reserving a portion of a pool bandwidth resource and invoking the CAC algorithm to additionally reserve a portion of the free bandwidth resource. The node proceeds to allocate the reserved pool bandwidth to the user in response to the acceptance message indicating that the same amount of the reserved pool bandwidth is available in the downstream node. The allocation of the pool bandwidth is temporary. When a portion of the free bandwidth resource is reserved using the CAC algorithm, this portion is exclusively allocated to the user until the end of the call and the temporarily allocated pool bandwidth is returned to the pool resource for other users.

15 Claims, 15 Drawing Sheets

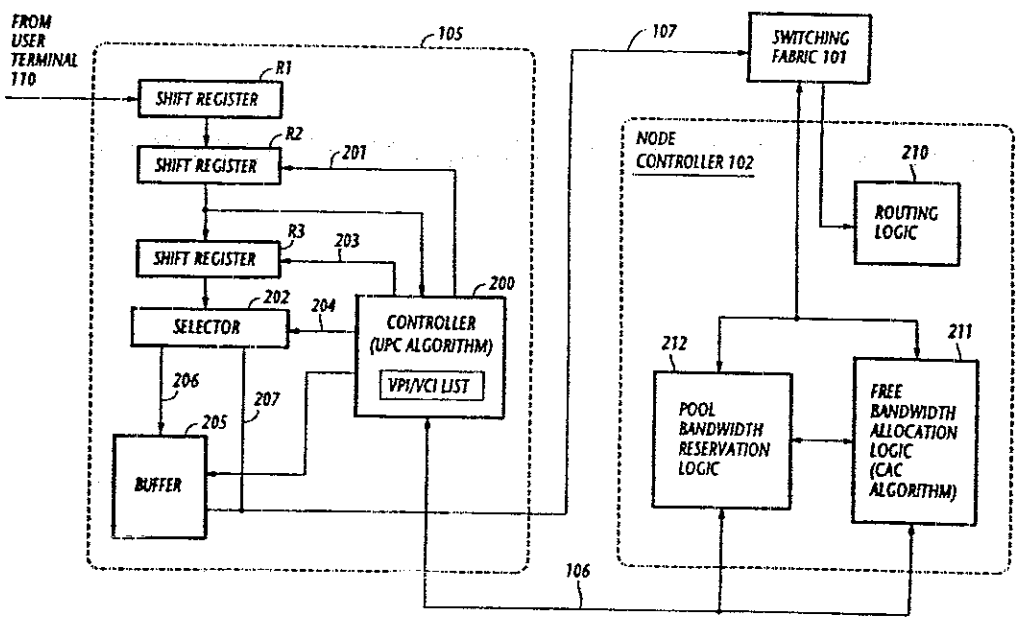
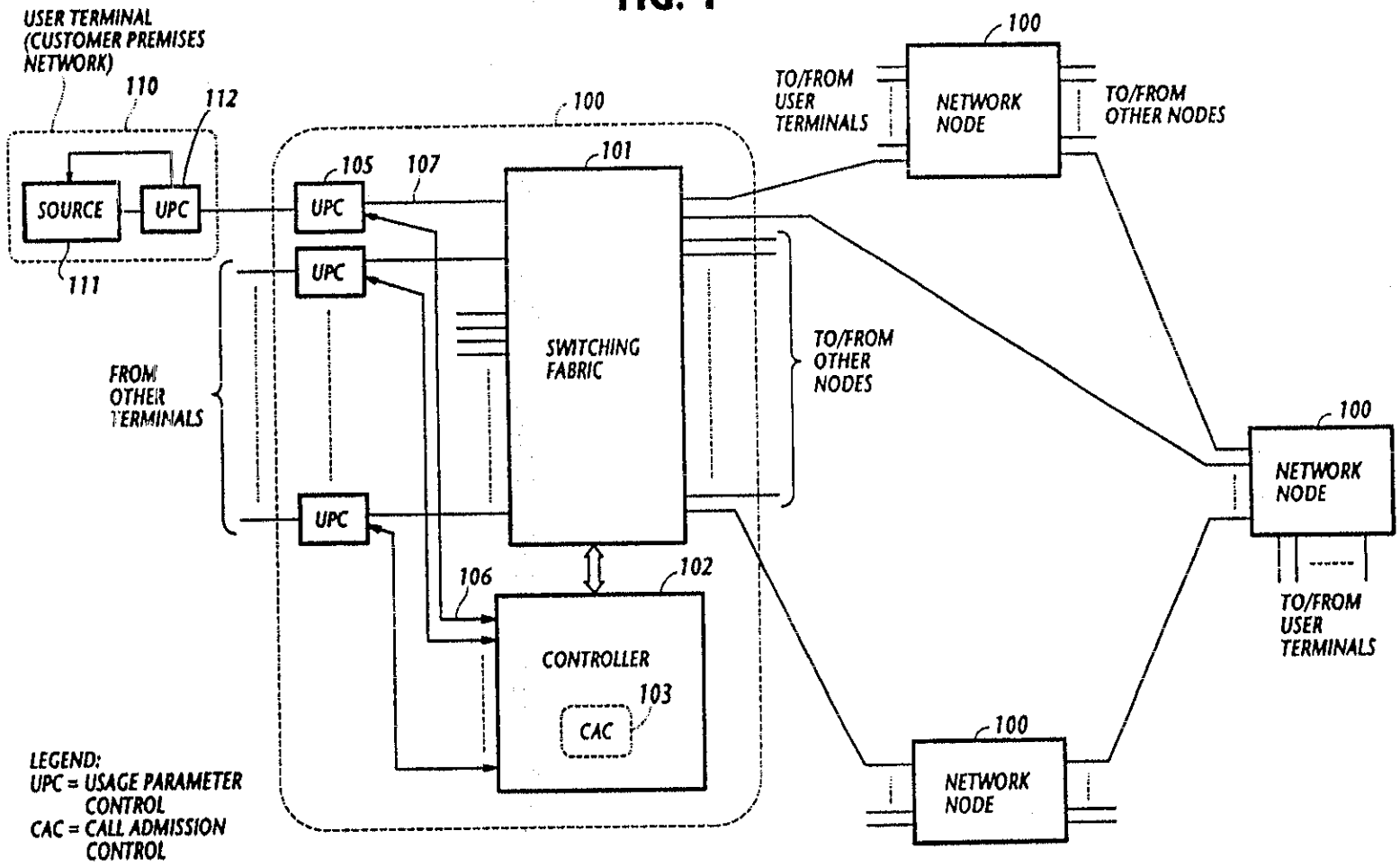


Exhibit 5

FIG. 1


USER TERMINAL (CUSTOMER PREMISES NETWORK)
110
112
SOURCE
UPC
111
100
105
107
UPC
UPC
UPC
FROM OTHER TERMINALS
101
SWITCHING FABRIC
TO/FROM OTHER NODES
106
102
CONTROLLER
103
CAC
LEGEND:
UPC = USAGE PARAMETER CONTROL
CAC = CALL ADMISSION CONTROL
TO/FROM USER TERMINALS
100
NETWORK NODE
TO/FROM OTHER NODES
100
NETWORK NODE
TO/FROM USER TERMINALS
100
NETWORK NODE

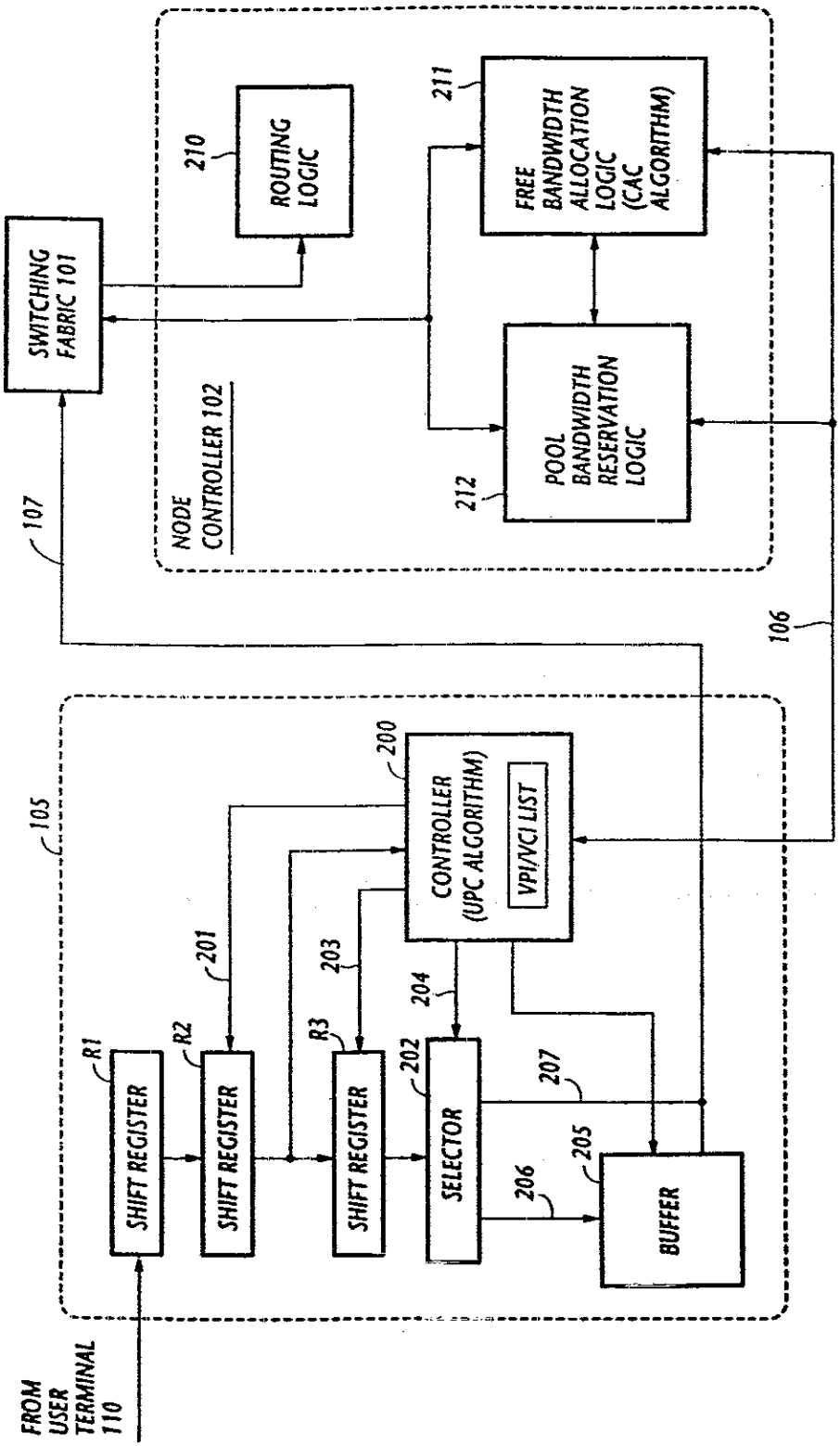
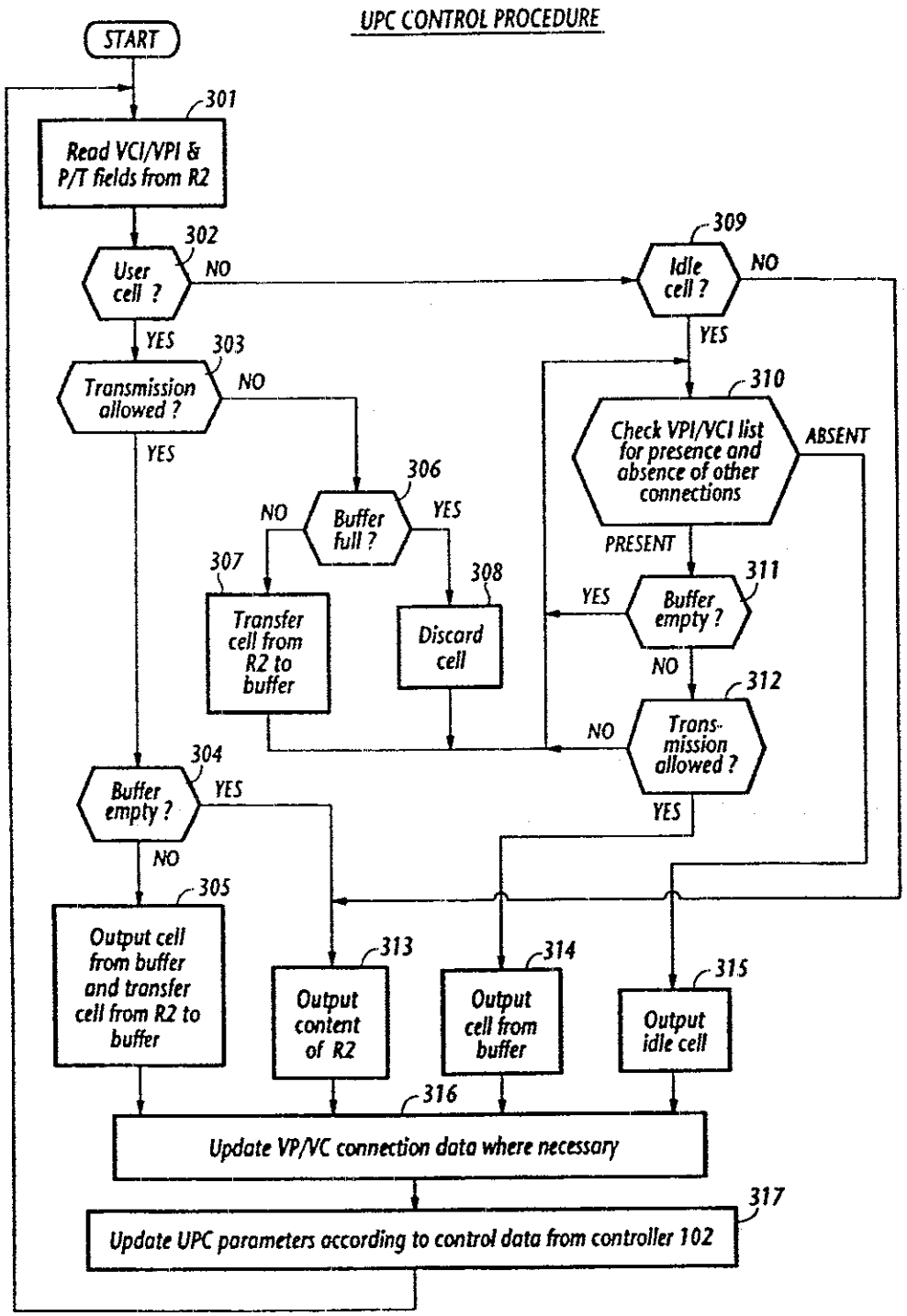

SWITCHING FABRIC 101
107
NODE CONTROLLER 102
210
ROUTING LOGIC
211
FREE BANDWIDTH ALLOCATION LOGIC (CAC ALGORITHM)
212
POOL BANDWIDTH RESERVATION LOGIC
106
105
200
CONTROLLER (UPC ALGORITHM)
VPI/VCI LIST
201
203
204
R1
R2
R3
202
207
205
206
SHIFT REGISTER
SHIFT REGISTER
SHIFT REGISTER
SELECTOR
BUFFER
FROM USER TERMINAL 110

FIG. 2

FIG. 3

UPC CONTROL PROCEDURE