UNITED STATES DISTRICT COURT
EASTERN DISTRICT OF TEXAS
LUFKIN DIVISION

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U.S. DISTRICT COURT
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MOTOROLA, INC., **Plaintiff,** **v.** **WINBOND ELECTRONICS CORPORATION, and WINBOND ELECTRONICS CORPORATION AMERICA,** **Defendants.**	**CIVIL ACTION NO.** 9:02cv10 **JURY TRIAL DEMANDED** Judge Hannah

COMPLAINT FOR DAMAGES AND INJUNCTIVE RELIEF

DEMAND FOR JURY TRIAL

Plaintiff Motorola, Inc., by its attorneys, complains against Winbond Electronics Corporation and Winbond Electronics Corporation America, and alleges as follows:

Parties

1. Plaintiff Motorola, Inc. ("Motorola"), is a corporation organized under the laws of the State of Delaware with its principal place of business at 1303 East Algonquin Road, Schaumburg, Illinois 60196. Motorola markets and sells semiconductor products throughout the United States, including within this District.

2. On information and belief, Defendant Winbond Electronics Corporation ("Winbond") is a corporation organized under the laws of Taiwan, the Republic of China, with its principal place of business at No. 4, Creation Road 3, Science-Based Industrial Park, Hsinchu, 300, Taiwan, R.O.C. Winbond manufactures semiconductor products in

Taiwan, imports its products into the United States and sells and/or offers for sale its products for importation into the United States. In addition, Winbond's semiconductor products are marketed, sold, and/or offered for sale throughout the United States, including within this District.

3. On information and belief, Defendant Winbond Electronics Corporation America ("Winbond America") is a corporation organized under the laws of the State of Delaware with its principal place of business at 2727 North First Street, San Jose, CA 95134. Winbond America imports, sells and/or offers for sale its products in the United States. In addition, Winbond America's semiconductor products are marketed, sold, and/or offered for sale throughout the United States, including within this District.

Jurisdiction and Venue

4. This is an action arising under the patent laws of the United States, 35 U.S.C. § 101 et seq. This Court has subject matter jurisdiction under 28 U.S.C. §§ 1331 and 1338(a).

5. Venue is proper in this judicial district under 28 U.S.C. §§ 1391(b), (c) and (d) and 1400(b).

The Patents

6. United States Patent No. 4,758,945, invented by James J. Remedi, entitled "Method for Reducing Power Consumed by a Static Microprocessor" (the "'945 Remedi Patent"), was duly and legally issued by the United States Patent and Trademark Office on July 19, 1988. A copy of the '945 Remedi Patent is attached hereto as Exhibit A.

7. United States Patent No. 4,468,411, invented by James W. Sloan, Truoc T. Tran, and Frank T. Jones, III, entitled "Method for Providing Alpha Particle Protection for an Integrated Circuit Die" (the "Sloan Patent"), was duly and legally issued by the United States Patent and Trademark Office on August 28, 1984. A copy of the Sloan Patent is attached hereto as Exhibit B.

8. United States Patent No. 4,446,194, invented by Jon Candelaria and Kurt S. Heidinger, entitled "Dual Layer Passivation" (the "Candelaria Patent"), was duly and legally issued by the United States Patent and Trademark Office on May 1, 1984. A copy of the Candelaria Patent is attached hereto as Exhibit C.

9. United States Patent No. 4,279,947, invented by Jon C. Goldman, Larry D. McMillan, and James B. Price, entitled "Deposition of Silicon Nitride" (the "Goldman Patent"), was duly and legally issued by the United States Patent and Trademark Office on July 21, 1981. A copy of the Goldman Patent is attached hereto as Exhibit D.

10. United States Patent No. 5,367,494, invented by Michael C. Shebanow, Mitchell K. Alsup, Hunter L. Scales, and George P. Hoekstra, entitled "Randomly Accessible Memory Having Time Overlapping Memory Accesses" (the "Shebanow Patent"), was duly and legally issued by the United States Patent and Trademark Office on November 22, 1994. A copy of the Shebanow Patent is attached hereto as Exhibit E.

11. United States Patent No. 4,794,434, invented by Perry H. Pelley, III, entitled "Trench Cell for a DRAM" (the "Pelley Patent"), was duly and legally issued by the United States Patent and Trademark Office on December 27, 1988. A copy of the Pelley Patent is attached hereto as Exhibit F.

12. United States Patent No. 4,511,914, invented by James J. Remedi, Don G. Reid, and Lynette Ure, entitled "Power Bus Routing for Providing Noise Isolation in Gate Arrays" (the "'914 Remedi Patent"), was duly and legally issued by the United States Patent and Trademark Office on April 16, 1985. A copy of the '914 Remedi Patent is attached hereto as Exhibit G.

13. Motorola is the owner of all rights, title and interest in and to the '945 Remedi Patent, the Sloan Patent, the Candelaria Patent, the Goldman Patent, the Shebanow Patent, the Pelley Patent, and the '914 Remedi Patent (collectively, the "Motorola Patents") and is entitled to sue for past and future infringement.

Background

14. The Motorola Patents cover inventions relating to semiconductor processing and semiconductor chip design.

15. The Defendants have imported into the United States, marketed, sold and/or offered for sale in the United States, products covered by the Motorola Patents.

16. The Defendants have had actual and/or constructive notice and knowledge of the Motorola Patents. The filing of this Complaint also constitutes notice in accordance with 35 U.S.C. § 287. Despite such notice, the Defendants continue to import into and sell in the United States products covered by the Motorola Patents.

Count I

17. Motorola repeats and realleges the allegations in paragraphs 1-16.

18. On information and belief, the Defendants have infringed, and/or induced infringement of, the '945 Remedi Patent by importing into, offering for sale, or selling in the United States, or by intending that others import into, offer for sale, or sell in the United States, products that incorporate the invention of, and/or were made using the methods claimed in, the '945 Remedi Patent.

19. On information and belief, the Defendants' infringement of the '945 Remedi Patent has been willful. Defendants' continued infringement of the '945 Remedi Patent has damaged and will continue to damage Motorola.

20. On information and belief, the Defendants' infringement of the '945 Remedi Patent has caused and will continue to cause Motorola irreparable harm unless enjoined by the Court. Motorola has no adequate remedy at law.

Count II

21. Motorola repeats and realleges the allegations in paragraphs 1-16.

22. On information and belief, the Defendants have infringed, and/or induced infringement of, the Sloan Patent by importing into, offering for sale, or selling in the United States, or by intending that others import into, offer for sale, or sell in the United

States, products that incorporate the invention of, and/or were made using the methods claimed in, the Sloan Patent.

23. On information and belief, the Defendants' infringement of the Sloan Patent has been willful. The Defendants' continued infringement of the Sloan Patent has damaged and will continue to damage Motorola.

24. On information and belief, the Defendants' infringement of the Sloan Patent has caused and will continue to cause Motorola irreparable harm unless enjoined by the Court. Motorola has no adequate remedy at law.

Count III

25. Motorola repeats and realleges the allegations in paragraphs 1-16.

26. On information and belief, the Defendants have infringed, and/or induced infringement of, the Candelaria Patent by importing into, offering for sale, or selling in the United States, or by intending that others import into, offer for sale, or sell in the United States, products that incorporate the invention of, and/or were made using the methods claimed in, the Candelaria Patent.

27. On information and belief, the Defendants' infringement of the Candelaria Patent has been willful. The Defendants' continued infringement of the Candelaria Patent has damaged and will continue to damage Motorola.

28. On information and belief, the Defendants' infringement of the Candelaria Patent has caused and will continue to cause Motorola irreparable harm unless enjoined by the Court. Motorola has no adequate remedy at law.

Count IV

29. Motorola repeats and realleges the allegations in paragraphs 1-16.

30. On information and belief, the Defendants have infringed, and/or induced infringement of, the Goldman Patent by importing into, offering for sale, or selling in the United States, or by intending that others import into, offer for sale, or sell in the United

States, products that incorporate the invention of, and/or were made using the methods claimed in, the Goldman Patent.

31. On information and belief, the Defendants' infringement of the Goldman Patent has been willful. The Defendants' continued infringement of the Goldman Patent has damaged and will continue to damage Motorola.

32. On information and belief, the Defendants' infringement of the Goldman Patent has caused and will continue to cause Motorola irreparable harm unless enjoined by the Court. Motorola has no adequate remedy at law.

Count V

33. Motorola repeats and realleges the allegations in paragraphs 1-16.

34. On information and belief, the Defendants have infringed, and/or induced infringement of, the Shebanow Patent by importing into, offering for sale, or selling in the United States, or by intending that others import into, offer for sale, or sell in the United States, products that incorporate the invention of, and/or were made using the methods claimed in, the Shebanow Patent.

35. On information and belief, the Defendants' infringement of the Shebanow Patent has been willful. The Defendants' continued infringement of the Shebanow Patent has damaged and will continue to damage Motorola.

36. On information and belief, the Defendants' infringement of the Shebanow Patent has caused and will continue to cause Motorola irreparable harm unless enjoined by the Court. Motorola has no adequate remedy at law.

Count VI

37. Motorola repeats and realleges the allegations in paragraphs 1-16.

38. On information and belief, the Defendants have infringed, and/or induced infringement of, the Pelley Patent by importing into, offering for sale, or selling in the United States, or by intending that others import into, offer for sale, or sell in the United

States, products that incorporate the invention of, and/or were made using the methods claimed in, the Pelley Patent.

39. On information and belief, the Defendants' infringement of the Pelley Patent has been willful. The Defendants' continued infringement of the Pelley Patent has damaged and will continue to damage Motorola.

40. On information and belief, the Defendants' infringement of the Pelley Patent has caused and will continue to cause Motorola irreparable harm unless enjoined by the Court. Motorola has no adequate remedy at law.

Count VII

41. Motorola repeats and realleges the allegations in paragraphs 1-16.

42. On information and belief, the Defendants have infringed, and/or induced infringement of, the '914 Remedi Patent by importing into, offering for sale, or selling in the United States, or by intending that others import into, offer for sale, or sell in the United States, products that incorporate the invention of, and/or were made using the methods claimed in, the '914 Remedi Patent.

43. On information and belief, the Defendants' infringement of the '914 Remedi Patent has been willful. The Defendants' continued infringement of the '914 Remedi Patent has damaged and will continue to damage Motorola.

44. On information and belief, the Defendants' infringement of the '914 Remedi Patent has caused and will continue to cause Motorola irreparable harm unless enjoined by the Court. Motorola has no adequate remedy at law.

Prayer for Relief

WHEREFORE, Motorola, Inc., respectfully requests that this Court enter judgment in its favor and grant the following relief:

A. Adjudge that the Defendants are infringing the Motorola Patents;

B. Adjudge that the Defendants' infringement of the Motorola Patents was willful, and that Defendants' continued infringement of the Motorola Patents is willful;

C. Enter an order preliminarily and permanently enjoining the Defendants from any further acts of infringement of the Motorola Patents;

D. Award Motorola damages in an amount adequate to compensate Motorola for the Defendants' infringement of the Motorola Patents, but in no event less than a reasonable royalty under 35 U.S.C. § 284;

E. Enter an order trebling any and all damages awarded to Motorola by reason of the Defendants' willful infringement of the Motorola Patents, pursuant to 35 U.S.C. § 284;

F. Enter an order awarding Motorola interest on the damages awarded and its costs pursuant to 35 U.S.C. § 284;

G. Enter an order finding that this is an exceptional case and award Motorola its reasonable attorneys' fees pursuant to 35 U.S.C. § 285; and

H. Award such other relief as the Court may deem appropriate and just under the circumstances.

DATED: January 15, 2002

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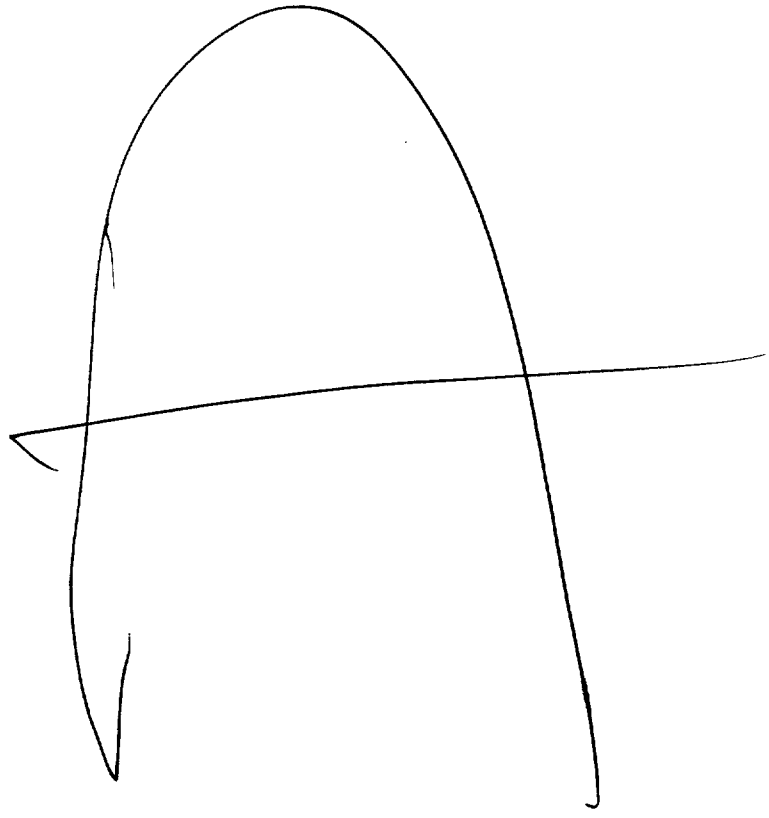

United States Patent [19]

Remedi

[11] **Patent Number: 4,758,945**

[45] **Date of Patent: Jul. 19, 1988**

[54] **METHOD FOR REDUCING POWER CONSUMED BY A STATIC MICROPROCESSOR**

[75] Inventor: **James J. Remedi**, Austin, Tex.

[73] Assignee: **Motorola, Inc.**, Schaumburg, Ill.

[21] Appl. No.: **65,292**

[22] Filed: **Aug. 9, 1979**

[51] **Int. Cl.**[4] **G06F 1/04**

[52] **U.S. Cl.** **364/200**

[58] **Field of Search** ... 364/200 MS File, 900 MS File; 365/227

[56] **References Cited**

U.S. PATENT DOCUMENTS

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3,535,560	10/1970	Cliff	364/200
3,736,569	5/1973	Bouricius et al.	364/200
3,855,577	12/1974	Vandierendonck	364/200
3,941,989	3/1976	McLaughlin et al.	235/156
4,030,079	6/1977	Bennett et al.	364/200
4,151,611	4/1979	Sugawara et al.	365/227
4,158,230	6/1979	Washizuka et al.	364/708
4,191,998	3/1980	Carmody	364/200

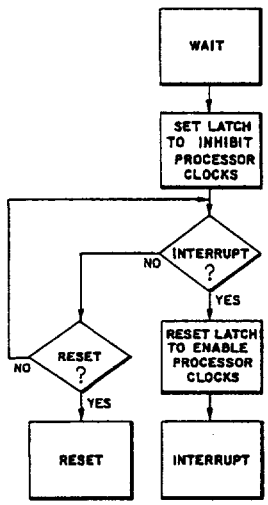
Primary Examiner—David Y. Eng

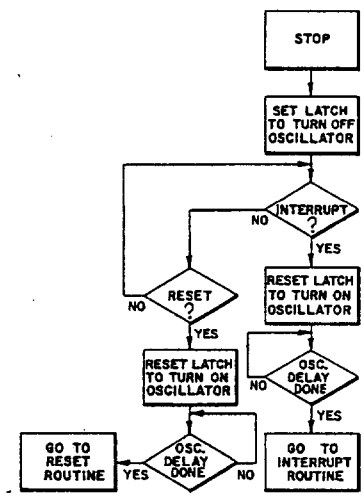
Attorney, Agent, or Firm—John A. Fisher; Jeffrey Van Myers

[57] **ABSTRACT**

In response to a software instruction, a static microprocessor is placed in a low current mode by disabling clock pulse generation. Means are provided for disabling a master oscillator when a STOP instruction is decoded. Additional means are provided for inhibiting clock pulses when a WAIT instruction is decoded without disabling the master oscillator. Clock pulse generation is again enabled upon receipt of a reset or interrupt signal.

6 Claims, 3 Drawing Sheets





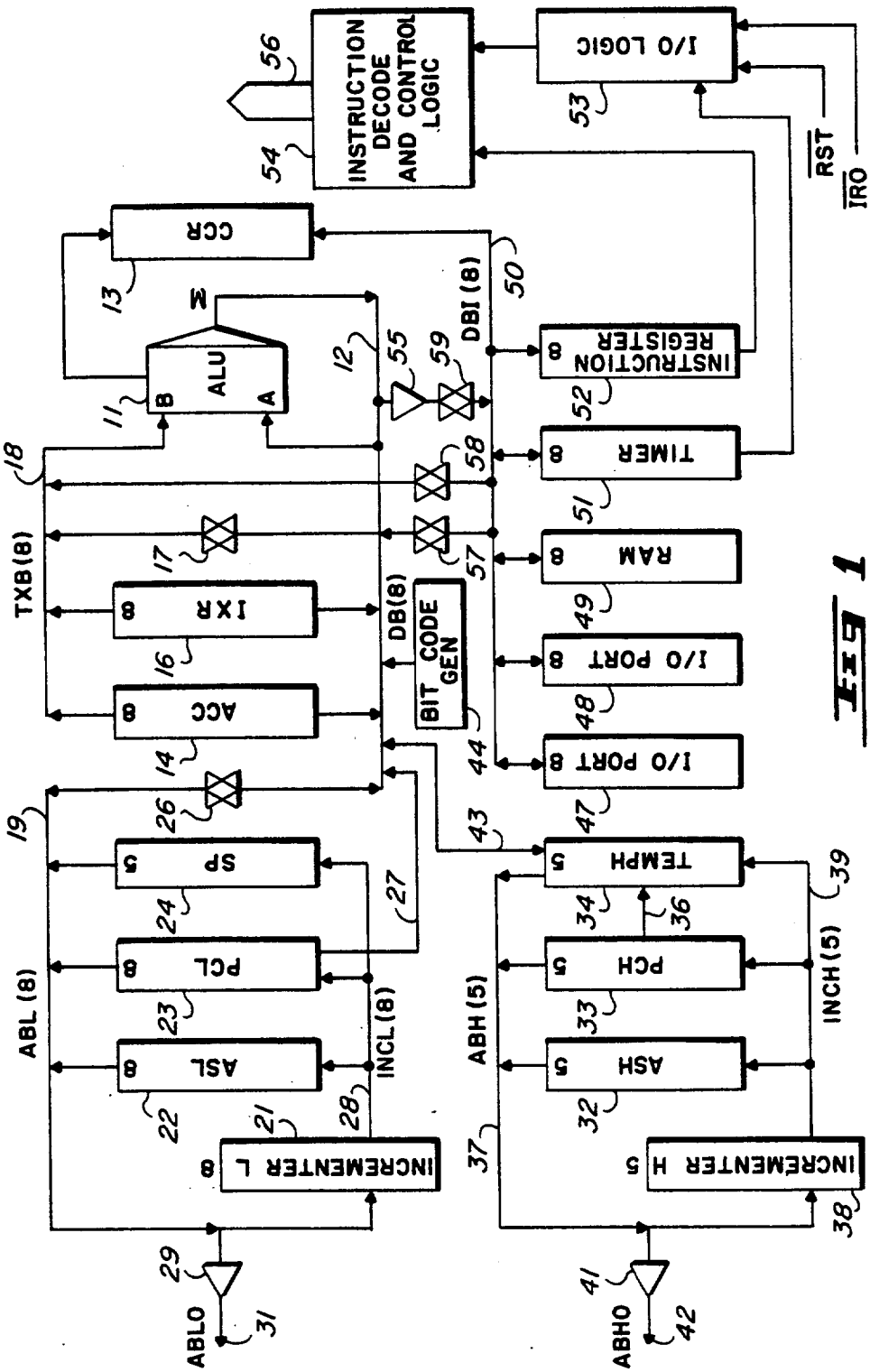

INSTRUCTION DECODE AND CONTROL LOGIC
I/O LOGIC
RST
IRQ
CCR
ALU
M
B
A
DBI (8)
INSTRUCTION REGISTER 8
TIMER 8
RAM 8
I/O PORT 8
I/O PORT 8
TEMPH 5
PCH 5
ASH 5
INCREMENTER H 5
INCH (5)
ABH (5)
ABHO
TXB (8)
IXR 8
ACC 8
DB(8)
BIT CODE GEN
SP 5
PCL 8
ASL 8
INCL (8)
ABL (8)
INCREMENTER L 8
ABLO

FIG. 1

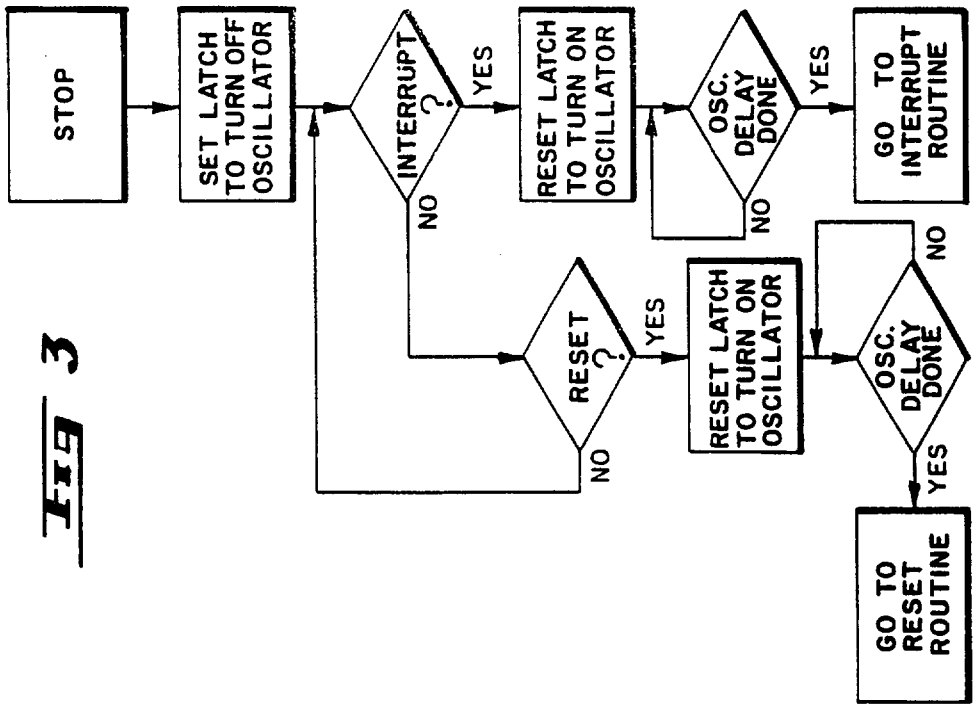

STOP
SET LATCH TO TURN OFF OSCILLATOR
INTERRUPT ?
YES
NO
RESET LATCH TO TURN ON OSCILLATOR
OSC. DELAY DONE
YES
NO
GO TO INTERRUPT ROUTINE
RESET ?
YES
NO
RESET LATCH TO TURN ON OSCILLATOR
OSC. DELAY DONE
NO
YES
GO TO RESET ROUTINE

Fig 3

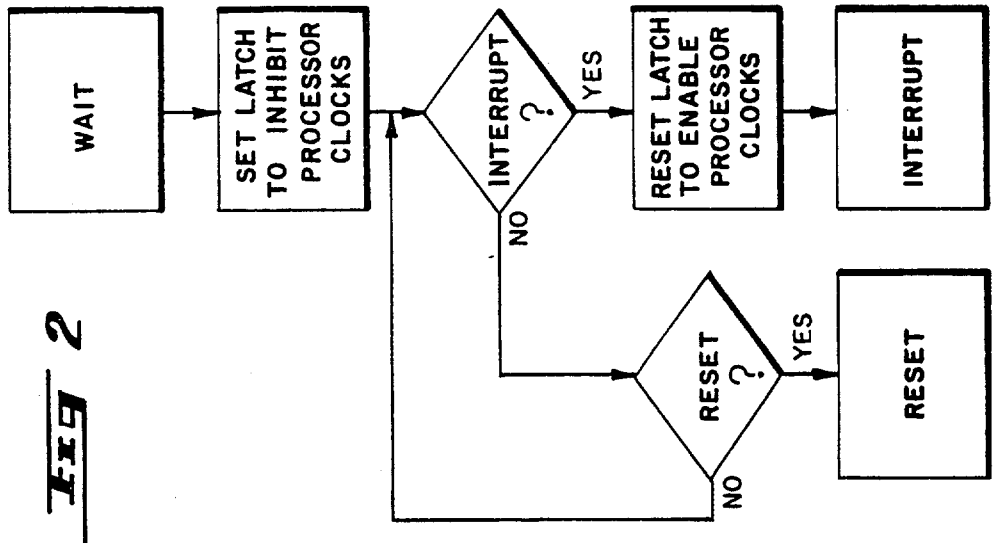

WAIT
SET LATCH TO INHIBIT PROCESSOR CLOCKS
INTERRUPT ?
YES
NO
RESET LATCH TO ENABLE PROCESSOR CLOCKS
INTERRUPT
RESET ?
YES
NO
RESET

Fig 2

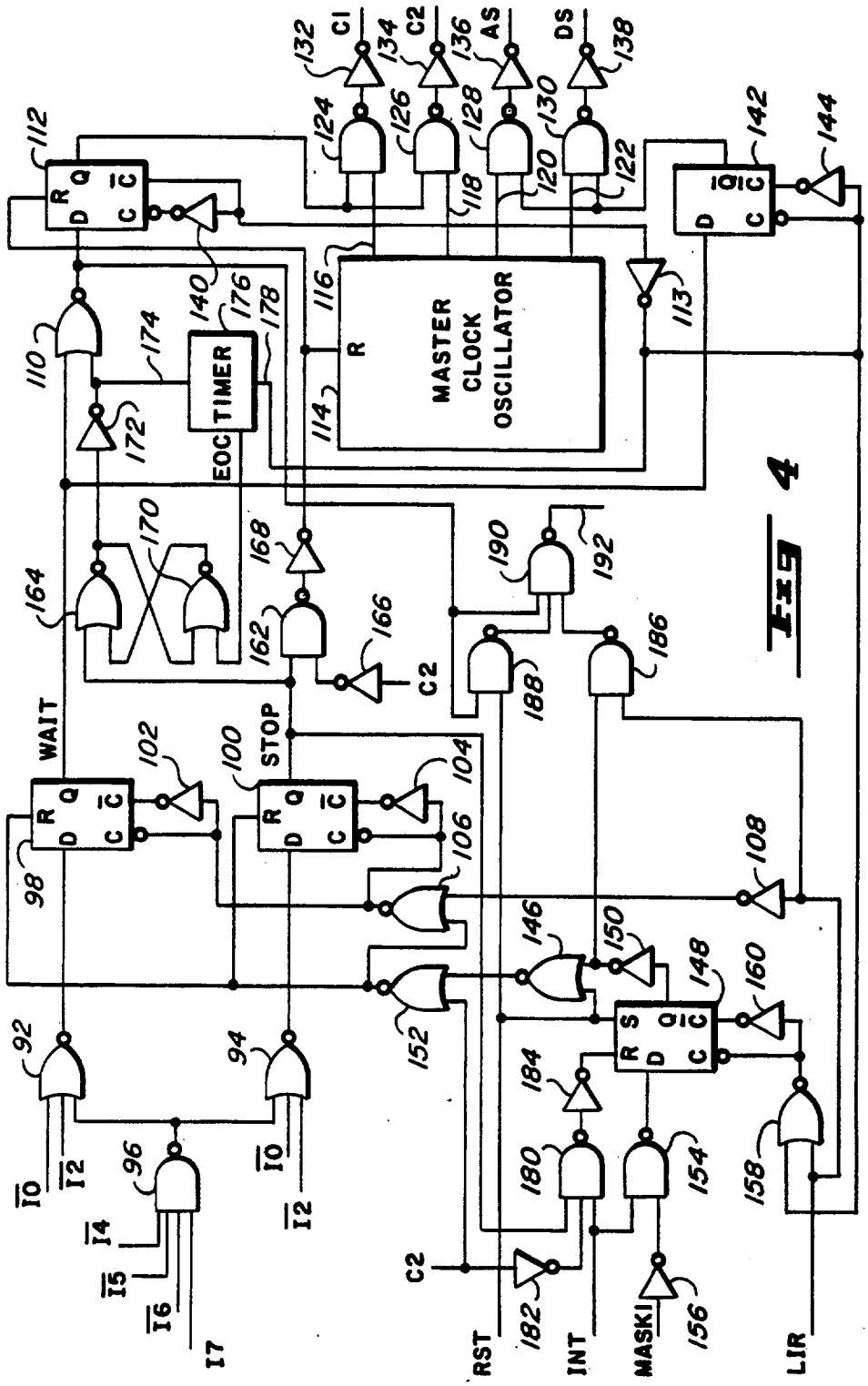

MASTER CLOCK OSCILLATOR
TIMER
EOC
WAIT
STOP
C1
C2
AS
DS
RST
INT
MASKI
LIR
I0
I2
I4
I5
I6
I7

FIG 4

METHOD FOR REDUCING POWER CONSUMED BY A STATIC MICROPROCESSOR

CROSS REFERENCE TO RELATED APPLICATIONS

(1) U.S. patent application Ser. No. 065,293 filed of even date herewith entitled "Apparatus for Reducing Power Consumed by a Static Microprocessor" and assigned to the assignee of the present invention.

(2) U.S. patent application Ser. No. 065,294 filed of even date herewith entitled "CMOS Microprocessor Architecture" and assigned to the assignee of the present invention.

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates generally to microcomputers and, more particularly, to a method for reducing the power consumed by static microprocessors.

2. Description of the Prior Art

Microcomputers are sophisticated, general purpose logic devices which can be programmed to perform a wide variety of useful control functions in industrial and communications equipment, large scale and medium scale computer peripheral and terminal hardware, automobiles and other transportation media, amusement and educational devices, household appliances and other consumer goods, and the like. Generally, an entire spectrum of microcomputers is presently available in the commercial marketplace. As the speed of operation increases, the more valuable and more versatile the microcomputer becomes since it is capable of controlling the given operation more efficiently and more accurately, of controlling a greater number of operations simultaneously, and of controlling operations requiring relatively fast response times.

The throughput of any given microcomputer is a function of, among other things, the number of machine cycles required to execute a given set of instructions. In the course of designing any computer system, and in particular a microcomputer, a set of instructions is selected which will provide the anticipated program requirements for the projected market in which the computer system is to be used. The microprocessor, or processor component of a single chip microcomputer, executes each instruction as a sequence of machine cycles, with the more complex instructions consuming a greater number of machine cycles.

The operation of the internal circuitry of the microprocessor is synchronized by means of a master clock signal applied to the microprocessor. The master clock signal may actually comprise two or even four clock components; i.e., the microprocessor clock may be two phase or four phase. During the basic clock cycle known as the machine cycle, a number of internal processor related operations may take place simultaneously including the transfer of digital information from a bus to a register or vice versa, between certain registers, from an address or data buffer to a bus or vice versa, and so forth. Additionally, the individual conductors of a bus may each be set to a predetermined logic level, or the contents of a register may be set to a predetermined logic level.

It is also desirable, particularly with respect to microcomputers intended for marketing in the middle to low end of the price scale, to minimize the computer chip size as much as possible.

Static microprocessors implemented with complementary MOS technology (CMOS) exhibits low DC current drain. Such systems are thus considered to consume less power and little power when operating. To further reduce power consumption, one known system utilizes a HALT instruction which inhibits processor execution. However, all clock signals utilized by the processor continue to be generated. Since a static microprocessor will maintain its state even in the absence of clock signals, it would be desirable to provide a method for disabling clock signals in an intelligent manner until further processor operations become necessary.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a method for reducing the power consumed by a static microprocessor.

It is a further object of the present invention to reduce power consumed by static microprocessor by utilizing software instructions which place the microprocessor in a very low current state.

It is yet another object of the present invention to provide a method for reducing power consumed by a CMOS static microprocessor by inhibiting the clock pulses generated until processor operation is required as indicated by some external stimulus.

According to a broad aspect of the invention there is provided a method for reducing, in response to at least one software instruction, energy consumed by a digital system of the type which includes a master oscillator having at least one signal output for producing a clock signal, said method comprising the steps of: decoding said at least one software instruction; and inhibiting said clock signal in response to said software instruction.

The above and other objects, features and advantages of the present invention will be more clearly understood from the following detailed description taken in conjunction with the accompany drawings; in which:

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a microprocessor in which the present invention may be embodied;

FIG. 2 is a flow diagram illustrating the sequence of operation produced by a WAIT instruction in accordance with the present invention;

FIG. 3 is a flow diagram illustrating the sequence of operation produced by a STOP instruction in accordance with the present invention; and

FIG. 4 is a logic diagram illustrating an apparatus for inhibiting clock signal in response to the WAIT or STOP instructions of FIGS. 2 and 3 to reduce power consumption in the processor.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to FIG. 1, there is shown a block diagram of a microprocessor of a type which may embody the present invention. The microprocessor includes a RAM, timer, and input/output (I/0). The microprocessor has an ALU 11 having an input A, an input B, and a summation output. The summation output is coupled to an 8 bit data bus 12. Data bus 12 couples information to input A. Information is carried to input B by an 8 bit transfer bus 18. An accumulator 14 is coupled to both transfer bus 18 and data bus 12. Accumulator 14 is an 8

bit general purpose register used for arithmetic calculations and data manipulations. An 8 bit index register 16 is coupled between transfer bus 18 and data bus 12. Index register 16 is used during an index mode of addressing and provides an 8 bit address which may be added as an offset to create a new effective address. Index register 16 is also used for calculations and data manipulation during read/modify/write instructions, and as a temporary storage register when not in use for addressing purposes. A transmission gate 17 is used to couple data bus 12 to transfer bus 18. A condition code register 13 is coupled to internal data bus 50 and receives an input from ALU 11. Condition code register 13 is a 5 bit register and contains flags which reflects the results of ALU 11 operations. A first bit contained in condition code register 13 is a carry bit and is set when a carry or a borrow out of ALU 11 occurs during an arithmetic operation. The carry bit can also be modified by certain branch instructions. A second bit in condition code register 13 is a zero bit and is set whenever the result of the last arithmetic, logical, or data manipulation is zero. A third bit is a negative bit which indicates that the result of the last arithmetic, logical, or data manipulation is negative. A fourth bit is a mask interrupt bit and when set, disables both external and timer interrupts. Clearing the interrupt mask bit enables both of the interrupts. Both the timer and external interrupts are latched so that no interrupts are lost because of the interrupt mask bit being set. A fifth bit is a half carry bit, and is set if a carry occurs between bits 3 and 4 of the ALU during an add or an add with carry instruction.

An 8 bit address bus 19 is coupled to data bus 12 by transmission gate 26. Address bus 19 carries the lower 8 bits of an address. The microprocessor of FIG. 1 is capable of addressing up to 8K bytes of external memory with a multiplexed address/data bus. Address bus 19 is coupled to an output buffer 29 and to an incrementer 21. Buffer 29 provides buffered outputs on line 31 which is the 8 bit lower order output address bus. Incrementer 21 is an 8 bit incrementer which can decrement as well as increment. Incrementer 21 is coupled to three registers by line 28. The three registers are an address store register 22, a program counter register 23, and a stack pointer 24. Address store 22 is an 8 bit register which is used to store a lower order effective address such as generated from a branch instruction. Program counter 23 is an 8 bit register which contains the lower 8 bits of a thirteen bit word which is used to point to the next instruction to be executed by the microprocessor. Stack pointer 24 is a 6 bit stack pointer which contains the address of the next free location on a push down/pop up stack. The stack pointer 24 decrements during pushs and increments during pulls. Stack pointer 24 is used to store the location of the return address on subroutine calls and to store the location of the machine state during interrupts. In a preferred embodiment stack pointer 24 is an 8 bit register with the two most significant bits permanently set to a predetermined state.

The outputs of registers 22, 23, and 24 are connected to address bus 19. Program counter 23 also provides an output to data bus 12 via line 27. When one of register 22, 23, or 24 is desired to be modified its contents are transferred by address bus 19 to incrementer 21, where incrementer 21 can increment or decrement the contents, and the contents are then carried by line 28 back to any desired register. This arrangement of incrementer 21 with registers 22, 23 and 24 permit one common incrementer/decrementer for three registers with one of the registers, the program counter 23, also being directly coupled to data bus 12. As mentioned hereinbefore, address bus 19 is coupled to data bus 12 by transmission gate 26.

It should be noted that although the buses are illustrated by one line that they are multiple lines with each different line carrying a different data bit.

The higher five bits of the address word is provided on line 42 by output buffer 41. Output buffer 41 is coupled to a 5 bit address bus 37. It should be noted that in a preferred embodiment, the lower eight bits of the address are multiplexed to external devices while the upper five bits are directly provided on interface pins. Address bus 37 is also coupled to an incrementer/decrementer 38 which is similar to incrementer 21 but only handles five bits. An address store register 32 is coupled from the output of incrementer 38 to address bus 37. Address store 32 contains the high bits of the address while address store 22 contains the lower eight bits of the address. A 5 bit program counter 33 is coupled between the output of incrementer 38 and address bus 37. A 5 bit temporary register 34 is coupled from the output of incrementer 38 to address bus 37. Program counter 33 also provides an output 36 to temporary register 34, which allows the contents of program counter 33 to be directly transferred into temporary register 34. This transfer between registers of course results in faster operation. The output of incrementer 38 is carried by a 5 bit bus or line 39 to registers 32, 33, and 34. Temporary register 34 is directly coupled to data bus 12 by interconnect bus 43. A bit code generator 44 is also connected to data bus 12 which allows any one of the bit lines of data bus 12 to be set or reset under instruction control.

An 8 bit internal data bus 50 is coupled by transmission gate 57 to data bus 12, by a transmission gate 58 to transfer bus 18, and receives information from data bus 12 by buffer/driver 55 and transmission gate 59. Buffer/driver 55 and transmission gate 59 are connected in series. As will be seen hereinafter, the registers are compact, fully static, and are not required to provide static current drive since the drive is provided by buffer 55. By having buffers/drivers 29, 41, and 55 the registers do not require large current drivers and therefore the entire microprocessor can be made smaller in size. An 8 bit I/0 port 47 and an 8 bit I/0 port 48 are coupled to internal data bus 50. I/0 ports 47 and 48 contain data direction registers which control whether the individual interface pins associated with the I/0 ports are serving as an input or an output for the microprocessor. Also coupled to internal data bus 50 is a random access memory (RAM) 49 which stores 8 bit words. In a preferred embodiment, RAM 49 stores 112 bytes. RAM 49 could be used for, among other things, a stack to store the contents of the registers during an interrupt.

Timer 51 is coupled to internal data bus 50 and has a single 8 bit counter with a 7 bit prescaler as its timer. The 8 bit counter is preset under program control and then decrements towards zero. When a zero crossing is detected the timer interrupt request bit of timer 51 is set, then, if a timer interrupt mask and the interrupt mask bit of condition code register 13 are both cleared the microprocessor receives an interrupt. The microprocessor now stores the appropriate registers on the stack, which is located in RAM 49, and then fetches the interrupt address vectors and begins servicing the interrupt. The prescaler of timer 51 is a 7 bit counter used to extend the maximum length of the timer. Timer 51 also provides an

output to input/output logic 53. Input/output logic 53 provides an output to instruction decode and control logic 54. Input/output logic 53 receives and processes a reset and an interrupt request input. An 8 bit instruction register 52 is coupled from internal data bus 50 to instruction decode and control logic 54. Control logic 54 provides decoded instruction outputs and the necessary controls on output lines 56. The outputs on line 56 are used throughout the microprocessor to control the functioning and operation of the microprocessor, a few of such being transmission gates 17, 57, 58, and 59 and bit code generator 44. It is possible for the microprocessor to be a microcomputer simply by the addition of a read only memory (ROM) coupled to internal data bus 50.

A detailed description of the microprocessor shown in FIG. 1 can be found in U.S. patent application Ser. No. 065,294 filed of even date herewith entitled "CMOS Microprocessor Architecture" and assigned to the assignee of the present invention.

As stated previously, a static CMOS microprocessor will maintain its state even in the absence of clock signals. Therefore, to reduce the amount of power consumed, it is desirable to inhibit clock pulses when the processor need not be functioning. This, according to the present invention, is accomplished in two ways. First, a WAIT instruction is added to the instruction repertoire. When executed, the master clock oscillator continues to function as does the timer 51 shown in FIG. 1. However, all other internal processor clocks are inhibited. Thus, the WAIT instruction places the processor in a low power state. The processor may be again rendered operational by (1) activating an external reset, or (2) the presence of an interrupt signal.

A second approach to inhibiting the clocks when the processor need not function is to provide a STOP instruction to the instruction repertoire. When a STOP instruction is executed, both the master clock oscillator and the internal clocks are inhibited. The processor is now in a very low current state; i.e., only leakage current is present. The processor is then restarted as a result of an external reset or interrupt signal; however, it is necessary to provide some period of delay to allow the oscillator to become stable.

FIG. 2 is a flow diagram which illustrates the execution of a WAIT instruction. After a WAIT instruction has been decoded, a latch is set which inhibits the processor clocks. Thus, the processor is placed in a low current mode and awaits either a reset signal or an interrupt signal. If a reset signal is received, the processor will execute a reset routine. If, on the other hand, an interrupt is received, the above referred to latch is reset to enable the processor clocks to commence and an interrupt routine to be executed.

FIG. 3 is a flow diagram illustrating the use of the STOP instruction. After the STOP instruction has been decoded, a second latch is set which turns off the master oscillator. This places the processor in a very low current mode until either a reset or an interrupt signal is received. If an interrupt or a reset signal is received, the second latch is reset to enable the master oscillator. In order to assure that the oscillator is functioning with sufficient logic swing and has settled with respect to frequency, a predetermined amount of delay is provided before the processor executes an interrupt or reset routine.

FIG. 4 is a logic diagram illustrating the apparatus for inhibiting the clocks or master clock oscillator in response to a WAIT or STOP instruction respectively. The instruction is decoded in decode and control logic 54 (FIG. 1), and the individual decoded instruction bits or the complements thereof are applied to gates 92, 94 and 96. The output of NOR gate 92 will be high when signals I0, I2, $\overline{I4}$, $\overline{I5}$, $\overline{I6}$ and I7 are at a logical "1" level. The output of NOR gate 94 will be high when signals $\overline{I0}$, $\overline{I2}$, $\overline{I4}$, $\overline{I5}$, $\overline{I6}$ and I7 are at a logical "1" level. A logical "1" at the output of NOR gate 92 will occur when a WAIT instruction has been decoded, and a logical "1" will appear at the output of NOR gate 94 when a STOP instruction has been decoded. D- type flip-flops 98 and 100 are employed to latch the WAIT and STOP commands respectively. Both flip-flops 98 and 100 are clocked by the output of NOR gate 106 which is applied to the C inputs of flip-flops 98 and 100 directly and which is applied to the $\overline{C}$ inputs of flip-flops 98 and 100 via inverters 102 and 104 respectively. The clocking of these flip-flops occurs at the trailing edge of a load instruction register (LIR) signal which is applied to inverter 108 the output of which is applied to a first input of NOR gate 106. As will be discussed below, the second input of NOR gate 106 is normally low thus permitting flip-flops 98 and 100 to be clocked at the trailing edge of the LIR signal.

The operation of the circuit shown in FIG. 4 will first be described with reference to a WAIT instruction; i.e. a logical "1" appearing at the D input of flip-flop 98. At the trailing edge of the load instruction register signal, flip-flop 98 will be clocked thus latching the WAIT instruction and producing a logical "1" at the Q output of flip-flop 98. This output is coupled to a first input of NOR gate 110 and, as a result thereof, a logical "0" appears at the output of NOR gate 110 and the D input of flip-flop 112.

The master clock oscillator 114 produces outputs 116, 118, 120 and 122 which after propagation through NAND gates 124, 126, 128 and 130 respectively and through inverters 132, 134, 136 and 138 respectively form first and second clock signals (C1 and C2), an address strobe (AS) and a data strobe (DS). Output 116 from master clock 114 is applied directly to the $\overline{C}$ input of flip-flop 112 and to the C input of flip-flop 112 via inverter 140. Therefore, after a logical "0" has been placed at the D input of flip-flop 112 in response to the latching of a WAIT instruction, the Q output of flip-flop 112 will become a logical "0" at the leading edge of the next clock pulse appearing at output 116. The Q output of flip-flop 112 is applied to inputs of NAND gates 124 and 126. Thus, when flip-flop 112 is in the zero state, NAND gates 124 and 126 do not permit passage of the signals appearing on master clock oscillator outputs 116 and 118. As a result, the outputs of inverters 132 and 134 remain a logical "0", and the processor clock pulses C1 and C2 are disabled.

The output of WAIT flip-flop 98 is also applied directly to the D input of flip-flop 142 which is clocked by the output of inverter 113. Thus, when a WAIT instruction is latched, flip-flop 142 is set at the next leading edge of the signal appearing on output 116. The $\overline{Q}$ output of flip-flop 142 is applied to inputs of NAND gates 128 and 130. Since the flip-flop 142 is now set, the $\overline{Q}$ output is a logical "0" thus inhibiting the passage of signals appearing on outputs 120 and 122 of the master clock oscillator. This produces a logical "0" at the output of inverters 136 and 138 thus disabling both the address strobe (AS) and the data strobe (DS) signals.

This is done to prevent the AS and DS lines from charging and discharging unnecessarily during the wait state.

The clock signals and address and data strobe signals will remain inhibited until either a reset signal (RST) or an interrupt signal (INT) is received. The reset signal RST is applied to a first input of NOR gate **146**. The output of flip-flop **148** after inversion in inverter **150** is applied to the second input of NOR gate **146**. Since flip-flop **148** is normally on, the output of inverter **150** will be a logical "0". Thus, when the reset signal (RST) goes high, a logical "0" will appear at the output of NOR gate **146**. This is applied to a first input of NOR gate **152**. Clock pulse C2 is applied to a second input of NOR gate **152**, and since this clock signal has been disabled as a result of the WAIT instruction, a logical "0" is applied to the second input of NOR gate **152**. This results in the production of a logical "1" at the output of NOR gate **152** and at the reset input of WAIT flip-flop **98**. With flip-flop **98** now reset, a logical "0" is applied to the D input of flip-flop **142** and a logical "1" is applied to the D input of flip-flop **112**. The next clock signal appearing on output **116** of master clock oscillator **114** will cause flip-flop **112** to set and flip-flop **142** to reset. This will enable NAND gates **124**, **126**, **128** and **130** resulting in the renewed production of clock signals C1 and C2, and address and data strobe signals AS and DS.

If, instead, an interrupt signal (INT), is applied to a first input of NAND gate **154**. A mask interrupt signal (MASKI) is applied to inverter **156** the output of which is coupled to a second input of NAND gate **154**. Thus, in the presence of an interrupt signal and in the absence of a mask interrupt signal, a logical "0" is applied to the D input of flip-flop **148**. Flip-flop **148** is clocked by the output of NOR gate **158** which is applied directly to the C input of flip-flop **148** and to the $\overline{C}$ input of flip-flop **148** via inverter **160**. The load instruction register signal (LIR) is applied to a first input of NOR gate **158** and the output of inverter **113** is applied to the second input. Thus, with a zero appearing at the D input of flip-flop **148**, the flip-flop is clocked by the next trailing edge of clock **116** resulting in a logical "0" at its Q output. This produces a logical "1" at the output of inverter **150** and a logical "0" at the output of NOR gate **146** since no reset signal is present. With logical "0's" at both inputs of NOR gate **152**, a logical "1" is applied to the reset input of WAIT flip-flop **98**. Clock signals C1 and C2 and address and data strobe signals AS and DS are again enabled as was described above in the case of a reset signal. It should be apparent that the primary purpose of flip-flop **148** is to synchronize the interrupt signal with the signal appearing on output **116** of the master clock oscillator **114**.

When a STOP instruction is decoded, a logical one is placed at the D input of STOP flip-flop **100**. This condition is latched by flip-flop **100** at the trailing edge of the load instruction register (LIR) signal as was described previously. The Q output of the STOP flip-flop **100** is applied to a first input of NAND gate **162** and a first input of NOR gate **164**. Clock signal C2 is inverted in inverter **166** and applied to a second input of NAND gate **162**. This synchronizes the output of NAND gate **162** with processor clock C2. When both of the Q output of STOP flip-flop **100** and the inverted processor clock C2 (i.e. $\overline{C2}$) are high, a logical "1" appears at the output of inverter **168**. This output is applied to a reset input of master clock oscillator **114** and to the reset input of flip-flop **112**. By resetting the master clock oscillator in this manner, outputs **116**, **118**, **120** and **122** are totally disabled.

The logical "1" at the output of STOP flip-flop **100** is also applied to one input of cross-coupled NOR gates **164** and **170**. A logical "0" will be produced at the output of NOR gate **164**, and a logical "1" will be produced at the output of inverter **172**. This produces a logical "0" at the D input of flip-flop **112**.

If a reset signal (RST) is received, a logical "1" will appear at the output of NOR gate **152** as was described previously. This output is coupled to the reset input of STOP flip-flop **100**. When flip-flop **100** becomes reset, a logical "0" will be applied to the reset input of master clock oscillator **114** thus enabling outputs **116**, **118**, **120** and **122**. However, flip-flop **112** has not yet been set and therefore clock signals C1 and C2 remain disabled. Since output **116** has been enabled, flip-flop **142** is clocked to a reset state thus enabling AS and DS.

Flip-flop **112** becomes set as follows. When the STOP flip-flop **100** was set, a logical "1" appeared at the output of inverter **172** which was applied via line **174** to timer **176**. This signal applied to timer **176** enables the timer to count clock pulses received from output **116** of master clock oscillator **114** over line **178**. Thus, when the STOP flip-flop **100** is reset, timer **176** begins counting pulses received over line **178**. When the counter in the timer reaches a predetermined state, an end of count (EOC) signal is applied to the input of NOR gate **170**. The EOC signal is a logical "1" which causes a logical "0" to appear at the output of gate **170** which is in turn applied to an input of NOR gate **164**. The output of STOP flip-flop **100** is likewise applied to an input of NOR gate **164**. Since the inputs to NOR gate **164** are both zero, the output of NOR gate **164** will be a logical "1" thus producing a logical "0" at the output of inverter **172**. With the zeros at both inputs of NOR gate **110**, a logical "1" is applied to the D input of flip-flop **112**. When the next pulse occurs on output **116** of master clock oscillator **114**, flip-flop **112** is clocked producing a logical "1" at its Q output. This now enables gates **124** and **126** to pass the signals appearing on outputs **116** and **118** to produce clock pulses C1 and C2.

Timer **176** may be employed to provide a delay of for example 2 milliseconds. Such timers are well known and a further discussion at this time is not deemed necessary. For example, the timer of U.S. Pat. No. 4,222,103 entitled "Real Time Capture Registers For Data Processor" and assigned to the assignee of the present invention would be suitable.

If instead of a reset signal, an interrupt signal should occur, it is still necessary to reset flip-flop **148**. However, since the master clock oscillator **114** has been disabled, no clock pulses can be applied to the C and $\overline{C}$ inputs of flip-flop **148**. Therefore, flip-flop **148** must be reset asynchronously. This is accomplished as follows, a logical "1" on the interrupt input is applied to a first input of NAND gate **180**. Since clock signal C2 is at a logical "0", a logical "1" is applied to a second input of NAND gate **180** via inverter **182**. Finally, a third input of NAND gate **182** is coupled to the output of STOP flip-flop **100** which, after execution of the STOP instruction, is at a logical "1" level. Therefore, the output of NAND gate **180** is at a logical "0" level. This output is inverted by inverter **184** and applied to the R input of flip-flop **148**. After flip-flop **148** is reset, the process is the same as above described resulting in the resetting of STOP flip-flop **100**.

One additional group of logic comprises NAND gates **186**, **188** and **190**. The first input of NAND gate **186** is coupled to the load instruction register (LIR) signal, and a second input is coupled to the output of inverter **150**. A first input of NAND gate **188** is coupled to the reset signal (RST) and a second input is coupled to the output of NOR gate **110** which is a logical "0" during a WAIT or STOP condition. The outputs of NAND gates **186** and **188** are respectively coupled to first and second inputs of NAND gate **190**. A third input of NAND gate **190** is coupled to the output of NOR gate **110**. The purpose of the output **192** of NAND gate **190** is to load the instruction register with a hardware interrupt thus making the system ready to receive an interrupt.

What is claimed is:

1. In a digital computing system which executes software instructions in synchronization with clock signals generated by a master clock oscillator in an enabled condition thereof, a method for reducing the energy consumed by the digital system, comprising the steps of:

decoding a predetermined software instruction selected for execution by said digital computing system;

inhibiting passage of said clock signals from said master clock oscillator to said digital computing system in response to the decoding of said predetermined software instruction, and continuing to inhibit passage of said clock signals for a predetermined length of time after said master clock oscillator has been enabled;

disabling the generation of said clock signals by said master clock oscillator in response to the decoding of said predetermined software instruction; and

enabling the generation of said clock signals by said master clock oscillator in response to a control signal.

2. A method according to claim **1** wherein said control signal comprises an externally produced reset signal.

3. A method according to claim **1** wherein said control signal comprises an interrupt signal.

4. In a digital computing system which executes software instructions in synchronization with clock signals generated by a master clock oscillator in an enabled condition thereof, a method for reducing the energy consumed by the digital system, comprising the steps of:

executing a predetermined software instruction selected for execution by said digital computing system;

inhibiting passage of said clock signals from said master clock oscillator to said digital computing system in response to the execution of said predetermined software instruction, and continuing to inhibit passage of said clock signals for a predetermined length of time after said master clock oscillator has been enabled;

disabling the generation of said clock signals by said master clock oscillator in response to the decoding of said predetermined software instruction; and

enabling the generation of said clock signals by said master clock oscillator in response to a control signal.

5. A method according to claim **1** wherein said control signal comprises an externally produced reset signal.

6. A method according to claim **1** wherein said control signal comprises an interrupt signal.

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United States Patent [19]

Sloan et al.

[11] **Patent Number: 4,468,411**

[45] **Date of Patent: Aug. 28, 1984**

[54] **METHOD FOR PROVIDING ALPHA PARTICLE PROTECTION FOR AN INTEGRATED CIRCUIT DIE**

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[73] Assignee: **Motorola, Inc.,** Schaumburg, Ill.

[21] Appl. No.: **365,724**

[22] Filed: **Apr. 5, 1982**

[51] **Int. Cl.**[3] **H01L 21/312;** H01L 23/00

[52] **U.S. Cl.** **427/8;** 427/5; 427/82; 427/378; 427/379; 427/385.5; 427/96

[58] **Field of Search** 427/5, 82, 96, 8, 378, 427/379, 385.5

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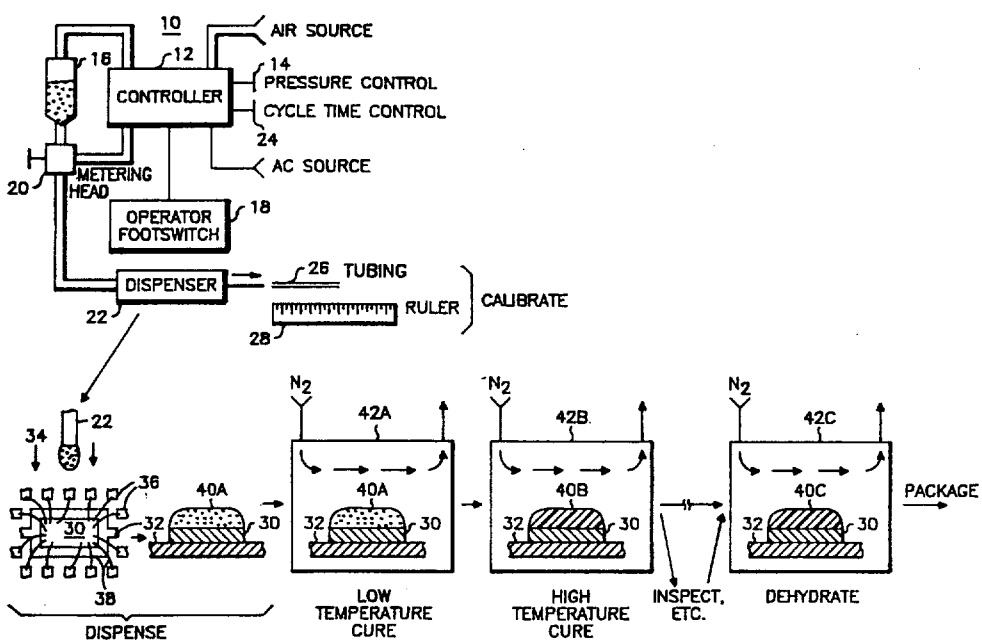
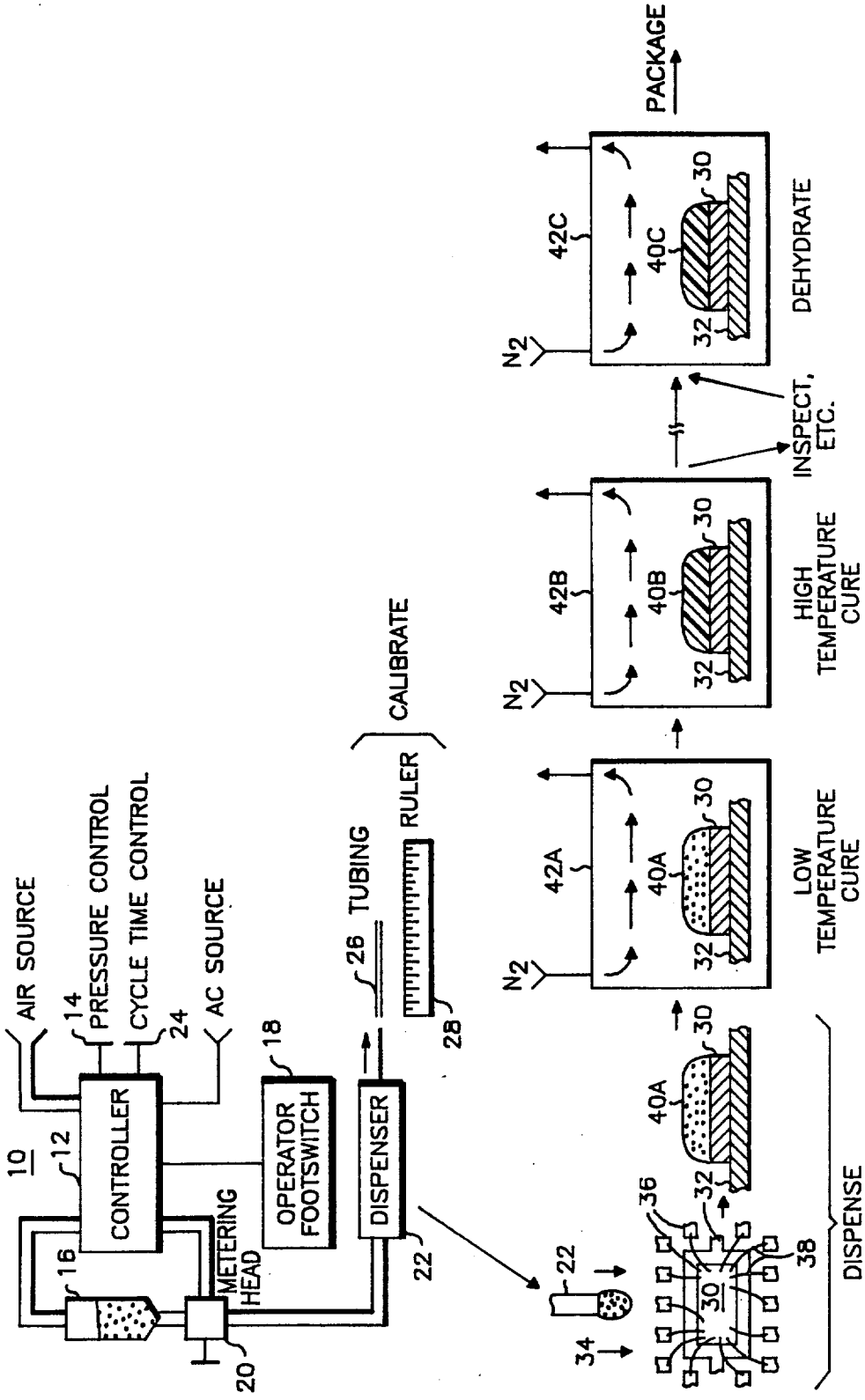
[57] **ABSTRACT**

A controlled quantity of a liquid polyimide precursor compound is deposited on the active surface of an integrated circuit die which has been prepared for packaging, and thereafter cured using a two step curing process to develop a polyimide coating of sufficient thickness to provide alpha particle protection for the die once packaged.

12 Claims, 1 Drawing Figure




10
12
CONTROLLER
14
AIR SOURCE
PRESSURE CONTROL
CYCLE TIME CONTROL
24
AC SOURCE
16
METERING HEAD
20
18
OPERATOR FOOTSWITCH
DISPENSER
22
26
TUBING
RULER
28
CALIBRATE
22
34
36
38
30
32
40A
DISPENSE
42A
40A
LOW TEMPERATURE CURE
42B
40B
HIGH TEMPERATURE CURE
INSPECT, ETC.
42C
40C
DEHYDRATE
PACKAGE
N2

METHOD FOR PROVIDING ALPHA PARTICLE PROTECTION FOR AN INTEGRATED CIRCUIT DIE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The subject invention relates generally to methods for providing alpha particle protection for integrated circuit die, and, in particular, to a method for providing alpha particle protection for an integrated circuit die prior to the plastic encapsulation thereof.

2. Description of the Prior Art

The phenomenon of charge carrier generation as a result of the passage of an alpha particle through the active surface of an integrated circuit die has been known for many years. However, the effects were generally considered to be laboratory curiosities prior to the advent of high density, dynamic MOS memories wherein the stored data is represented by the presence or absence of quantities of charge stored on capacitor portions of the storage cells. As improvements in fabrication processes allowed the shrinkage of the storage cells, the quantity of charge distinguishing a "zero" from a "one" shrank relative to the number of charge carriers generated by a typical alpha particle impact. In April of 1978, T. C. Mays and M. H. Woods with the physical analysis laboratory of Intel Corporation first reported the protection of "soft" errors induced by alpha particles in such dynamic memories. (*Proceedings of the* 1978 *International Reliability Physics Symposium;* see also "Alpha-Particle-Induced Soft Errors in Dynamic Memories," *I.E.E.E. Transactions on Electron Devices,* Vol. EE-26, January 1979).

Since 1978, efforts to prevent alpha particle induced errors in integrated circuits have focused on three approaches: (1) to design the circuitry, particularly charge storage cells, with sufficiently high operating margins to ensure that the quantity of charge carriers generated by even very energetic alpha particles will be insufficient to effect the logic state; (2) packaging the integrated circuit using materials having very low levels of radioactive impurities such as uranium and thorium; and (3) protecting the active surface of the integrated circuit with a material which absorbs the alpha particles before they reach the surface. A fourth alternative, not available to the integrated circuit manufacturer, is to provide an error detection and correction in the system in which the sensitive circuit is used. Since alternative 1 typically requires an increased charge storage capability, the resulting increase in die size will often be prohibitive. Alternative 2, while appearing to be the most advantageous, is very difficult to achieve and, with respect to plastic encapsulation, is presently unavailable due to the lack of any suitable filler material with sufficiently low levels of contaminants. As a result of these and other limitations, attention has been focused upon alternative 3 in an effort to identify one or more techniques for shielding the surface of the integrated circuit from the alpha particles generated within the package material itself.

In general, surface shielding has taken one of two forms: (1) a preformed tape of a suitably dense flexible material, such as polyimide, which can be adhered to the active surface of the integrated circuit prior to packaging; and (2) a liquid material, such as a liquid polyimide precursor compound, which is dispensed upon the active surface of the die and allowed to spread over

the critical area and then cured prior to packaging. Development of the tape process has been severely impacted by the difficulty in physically attaching the tape to the integrated circuit die without damaging either the die, the tape or the wire bonds connecting the circuit to the adjacent portions of the lead frame, and by difficulty in achieving consistant adhesion between the tape and the die so as to preclude separation during and after packaging. With respect to the liquid coating process, problems include poor coating to die surface adhesion as a result of improper formulation or contaminated die surfaces, insufficiently thick coating after curing to intercept alpha particles, and excessively thick coatings after curing resulted in shrink-induced separation or damage to the wire bonds or to die itself. However, at least one manufacturer, Hitachi Semiconductor Division of Japan, is currently marketing 64 K memory devices having a polyimide coating applied by a proprietary process using a liquid polyimide precursor compound currently marketed by the Hitachi Chemical Company of Japan. However, the Hitachi Chemical Company polyimide compound, while generally suitable for use in side braze packages, is generally unsuitable for use in hermetic cerdip packaging due to the intolerance of the required seal temperatures and the tendency to generate intolerable levels of internal cavity moisture. In addition, Hitachi Chemical Company offers no polyimide compound suitable for use of an integrated circuit die to be plastic encapsulated.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide a method for providing alpha particle protection for an integrated circuit die to be encapsulated in side braze, cerdip or plastic, as desired.

Another object of the present invention is to provide a method for dispensing a selected quantity of a liquid polyimide compound to provide alpha particle protection for an integrated circuit die.

These and other objects of the present invention are achieved in a method for providing alpha particle protection for an integrated circuit die which has been mounted on and electrically connected to a suitable lead frame, comprising the steps of: depositing a selected quantity of a liquid polyimide precursor compound having a predetermined solids content and viscosity on the active surface of the die to form a liquid polyimide precursor coating thereon; curing the coating for a first time period at a temperature selected to reduce the volatile content thereof below a predetermined level, and then for a second time period at a temperature selected to substantially complete the imidization thereof and the removal of the remaining volatile content thereof; and, substantially immediately prior to encapsulating the coated die and selected adjacent portions of the lead frame, dehydrating the coating for a third time period at a temperature selected to remove moisture absorbed by the coating since the curing thereof if a significant period of time has elapsed since the curing of the coating.

To achieve a coating of consistent thickness, a method is provided for dispensing a selected quantity of the liquid coating material onto the active surface of the integrated circuit die, comprising the steps of: subjecting to a substantially constant, predetermined pressure a quantity of a liquid polyimide precursor compound having a predetermined solids content and viscosity;

and then directing for a predetermined length of time a portion of said compound through a conduit of predetermined cross-sectional area onto said surface.

DESCRIPTION OF THE DRAWING

The single FIGURE illustrates the several steps comprising the method of the subject invention.

DESCRIPTION OF THE PREFERRED METHOD

In the development of the preferred method of the subject invention, considerable testing was done in order to determine the minimum thickness below which protection against the alpha particle radiation is insufficient to ensure that alpha particle induced soft errors during operation of the protected integrated circuit remained below a specified limit. In general, this minimum thickness is a function of the sensitivity of the integrated circuit to be protected, the selected soft error tolerance limit, the flux density and energy distribution of the alpha particle radiation emanating from the packaging materials, and the resistivity of the selected coating material after curing to the passage of alpha particles therethrough. For example, using the 64 K dynamic RAM integrated circuit commercially available from Motorola in a plastic package as part no. MCM6665AP, the Dupont polyimide precursor commercially available as Pyralin PI2562 satisfies a soft error tolerance limit of 1 failure in 10,000 hours with a minimum thickness of 1 mil. However, testing of cured coatings of other polyimide precursor compounds have been shown to exhibit similar alpha radiation shielding properties. While in general, coatings thicker than the minimum thickness provide extra insurance against alpha particle induced soft errors, shrinkage of the coating during the curing process may exert sufficient stress upon the die to cause wire bond separation or, under extreme circumstances, die shear or coating separation. Tests have shown that a maximum thickness of the cured coating of the order of about 10 mils should preclude such damage.

Having established a minimum and a maximum thickness goal for the cured coating appropriate for providing the desired level of alpha particle protection for a particular integrated circuit die, the viscosity and solids contents of an appropriate liquid polyimide precursor compound must be selected, since each affects the volume of compound necessary to produce the desired coating. In general, the viscosity of the selected liquid polyimide precursor compound must be low enough so that, when dispersed on the active surface of the integrated circuit die, it will flow outward to the die edges and completely cover the active surface. On the other hand, the viscosity must not be so high that the polyimide precursor compound will flow over the edges of the die, possibly contaminating other portions of the die assembly. Within these broad guidelines, a viscosity of the order of between about 75 and 200 centipoise has been found to be acceptable, although viscosities outside of this range may be acceptable from a functional standpoint in particular circumstances. While viscosity affects the surface coverage characteristic of the liquid polyimide precursor compound, the solids content or percent of solids in the compound tends to affect the cross sectional configuration of the final cured coating. For example, liquid polyimide precursor compounds containing less than about 15 percent solids have been found to produce a cured coating having a concave profile, thus undesirably thinning the cured coating over the central portions of the integrated circuit die. On the other hand, a liquid polyimide precursor compound having a solids content above about 30 to 37 percent tends to a viscosity higher than desired, thus requiring such a large amount of liquid material to completely cover the die that the resulting coating is excessively thick. As a result, the mismatch of the coefficients of thermal expansion between the die and the coating often generates shear stress between the die and the coating sufficient to cause delamination or die fracture. Thus, a suitable liquid polyimide precursor compound will have a percents solids between about 20 and 30 percent and, preferably, between about 24 and 27 percent.

An initial estimate of the volume of the selected liquid polyimide precursor compound required to provide the desired cured coating thickness may be computed in a conventional manner using the solids/solvents ratio of the selected compound and the active surface area of the integrated circuit die to be protected. Using this estimate as the starting point, more accurate determinations of the required volume can be empirically determined using the actual die and curing process. Recalibration for the particular die should thereafter be necessary only if the composition of the selected compound varies or if the curing process is modified.

In the preferred process for practicing the present integrated circuit protection method shown in the FIGURE, a precision fluid dispensing system **10** of the pneumatic type is employed. In the system **10**, a controller **12** is coupled in a conventional manner to a compressed air source (not shown) and to an alternating current source (not shown). In operation, the controller **12** applies a substantially constant pressure selected via a pressure control knob **14** to a reservoir **16** containing a quantity of the selected liquid polyimide precursor compound. In response to the actuation of an operator footswitch **18**, the controller **12** enables a metering head **20** to pass the pressurized polyimide precursor compound from the reservoir **16** to a hand-held dispenser **22** for a period of time determined by a cycle time control knob **24**. One such precision fluid dispensing system **10** suitable for practicing the present method is the model 280J commercially available from the Tridak Division of Indicon Inc., Secor Road, Brookfield Center, Conn. 06805.

To calibrate the selected dispensing system **10**, the pressure control knob **14** is set within the operating range of the controller **12** to suit the viscosity of the selected liquid polyimide precursor compound. The cycle time control knob **24** is then varied until the required volume is dispensed via the metering head **20**. Periodically, the accuracy of the volume dispensed by the dispensing system **10** can be quickly verified by inserting the dispensing needle portion of the dispenser **22** into a short section of tubing **26** having substantially the same inner diameter as the outer diameter of the dispensing needle. The resulting length of the column of liquid polyimide precursor injected into the tubing **26** will then be equal to the polyimide precursor actually dispensed divided by the cross-sectional area of the tubing **26**. This "gauge" length can be quickly verified using a ruler **28** or the like.

The present method is preferably performed after a given integrated circuit die **30** has been mounted for packaging, such as on the flag **32** of a conventional lead frame **34**, and electrically connected to the appropriate conductor leads **36** via bonding wires **38**. The dispens-

ing system **10** can then be selectively actuated via the operator footswitch **18** to deposit the selected quantity of the liquid polyimide precursor compound on the active surface of the die **30** to form a liquid polyimide precursor coating **40a** thereon. The die assembly is then placed in an oven **42a** and heated to a temperature selected to reduce the solvent content of the coating **40a** sufficiently slowly to preclude the formation of significant gas bubbles therein. For example, an upper temperature limit for this "low temperature cure" suitable for the PI2562 polyimide precursor has been found to be between about 100° C. and 150° C. However, it is deemed preferable to operate the oven **42a** somewhat below the particular upper temperature limit to minimize the likelihood of bubble generation, even though to do so may extend slightly the low temperature curing time. This low temperature cure should be continued until at least about 95% of the solvent content of the coating **40a** has been driven off, typically between about 1 and 4 hours. It has been discovered that the temperature of the oven **42a** should be ramped from about ambient up to the selected low cure temperature, in order to minimize the likelihood of delamination of the coating **40a** during the subsequent high temperature cure thereof. This can be accomplished directly by using a suitably equipped oven **42a** or indirectly by simply overloading an oven **42a** capable of bringing the overload up to the desired temperature within about 15 to 30 minutes of loading. One oven found particularly well suited for performing the low temperature cure using the latter indirect ramping technique is the Model 5851 commercially available from the National Appliance Company of Portland, Oreg.

After the low temperature cure, the partially cured coating **40b** is then raised to a temperature selected to substantially complete the imidization thereof and the removal of the remaining solvent content thereof and the water molecules released during the imidization process. The lower temperature limit for this "high temperature cure" should be sufficient to sustain the imidization process, while the upper temperature limit is generally dictated by the tolerance of the die assembly. A suitable temperature for performing this high temperature cure for the PI2562 polyimide precursor is between about 250° C. and 450° C., and preferably between about 300° C. and 350° C. A curing time between about 1 and 4 hours has been found suitable when using the latter preferred temperature range. Although the oven **42b** used to perform the high temperature cure may be the same as the oven **42a** used to perform the low temperature cure, the time consumed in temperature ramping may be saved by using different ovens. An oven found suitable for performing the high temperature cure is the model POM256-B.1 commercially available from the Blue M Electric Company of Blue Island, Ill.

To facilitate the removal of all of the solvents from the coating **40a–40b**, each of the ovens **42a** and **42b** should be plumbed with nitrogen (N_2) so that a flow of dry nitrogen can be maintained therethrough during both the low temperature cure and the high temperature cure. However, if the die assembly is of the ceramic type and the selected high cure temperature exceeds the melting point of the glass material in the package, dry filtered air is preferred rather than nitrogen in order to minimize migration of the lead plating material.

After the high temperature cure, the die **30** and particularly the coating **40c** thereon, should be inspected to identify any significant mechanical defects in the die **30** or the coating **40c**. Those die assemblies which exhibit die sheer or fracture, wire bond separation or shorting, or similar defects should be eliminated from further processing to minimize expense. Such an inspection should preferably be conducted under a laminar flow hood using a suitable microscope (not shown).

Although it is known that the cured polyimide coating **40c** is hygroscopic, it has been discovered that the rate of moisture absorption following the high temperature cure proceeds surprisingly rapidly. Tests have shown that after only 2 hours following the high temperature cure, the coating **40c** may absorb a sufficient amount of moisture from the ambient atmosphere to adversely affect the environment around the integrated circuit die **30** once packaged. Accordingly, in the preferred method, the coating **40c** is dehydrated in an oven **42c** at a temperature selected to remove any moisture absorbed by the coating **40c** since the curing thereof, substantially immediately prior to the packaging of the coated integrated circuit die **30** whether in plastic as shown in the FIGURE, or in ceramic. For the PI2562 polyimide precursor, a dehydration temperature between about 280° C. and 450° C. has been found suitable, so long as the drying time is at least about 10 minutes. The oven model POM256-B.1 commercially available from the Blue M Electric Company has been found suitable for performing the pre-packaging dehydration of this coating **40c**. As in the low temperature cure and the high temperature cure, it is preferred to provide a continuous flow of dry nitrogen, or air in the case of a ceramic package, through the oven **42c** during the dehydration to insure rapid removal of the moisture driven out of the coating **40c**.

Since many changes and modifications may be made to the several steps of the methods disclosed herein without departing from the spirit and scope of the present invention, it is therefore intended that the following claims cover all such changes and modifications.

I claim:

1. A method for providing alpha particle protection for an integrated circuit die which has been mounted for packaging and electrically connected to conductor leads integral with such packaging, comprising the steps of:

depositing a selected quantity of a liquid polyimide precursor compound having a predetermined solids content and viscosity on the active surface of the die to form a liquid polyimide precursor coating thereon;

curing the coating for a first time period at a first temperature selected to reduce the volatile content thereof below a predetermined level, and for a second time period at a second temperature selected to substantially complete the imidization thereof and the removal of the remaining volatile content thereof; and

substantially immediately prior to packaging the coated die, dehydrating the coating for a third time period at a third temperature selected to remove moisture absorbed by the coating since the curing thereof.

2. The method of claim **1** wherein the step of curing the coating for a first time period is performed at a first temperature selected to reduce the volatile content thereof below said predetermined level sufficiently slowly to preclude the formation of significant gas bubbles therein.

3. The method of claim 2 wherein said first time period comprises until at least about 95% of the solvent content of said coating has been driven off.

4. The method of claim 1 or 2 further including the step of:

inspecting the die and the coating thereon after the curing thereof to identify any significant mechanical defects in the die and coating; and

wherein the step of dehydrating the coating is performed after the inspection of the die and the coating thereon.

5. The method of claim 1 or 2 wherein the step of depositing said selected quantity of said liquid polyimide precursor compound comprises the steps of:

subjecting to a substantially constant, predetermined pressure a quantity of said liquid polyimide precursor compound; and

directing for a fourth predetermined length of time a portion of said compound through a conduit of predetermined cross-sectional area onto said surface.

6. The method of claim 5 including the further step of:

periodically dispensing one of said portions of said compound into a length of tubing of predetermined cross-sectional area and verifying that the resulting length of the column of said compound in said tubing is substantially equal to a predetermined gauge length.

7. The method of claim 1 or 2 wherein said first temperature is selected between about 100° C. and 150° C.

8. The method of claim 1 or 2 wherein said second temperature is selected between about 250° C. and 450° C., and preferably, between about 300° C. and 350° C.

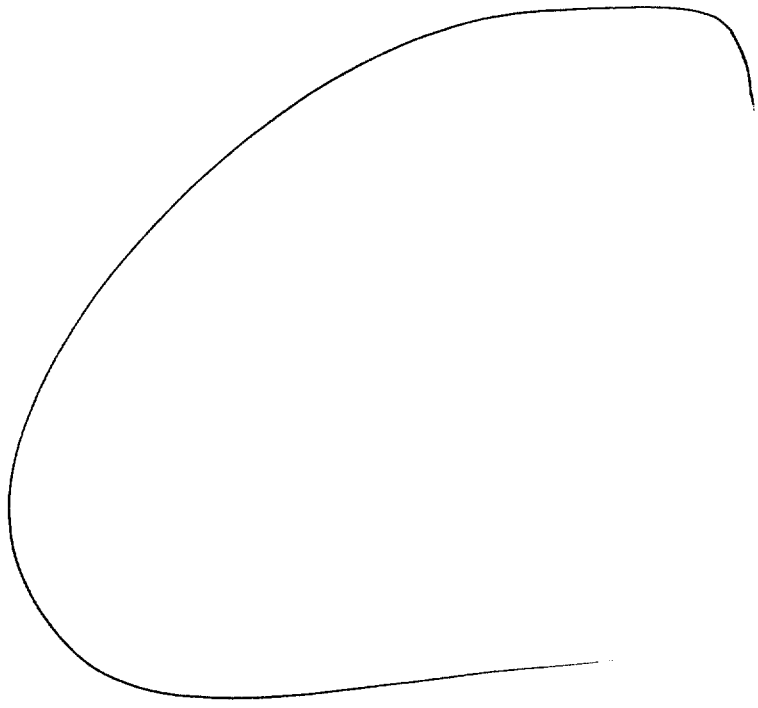
9. The method of claim 1 or 2 wherein the step of curing the coating is performed in a flow of dry nitrogen.

10. The method of claim 1 or 2 wherein the step of dehydrating the coating is performed in a flow of dry nitrogen.

11. The method of claim 1 or 2 wherein the liquid polyimide precursor compound has a solids content between about 20 and 30 percent, and preferably between about 24 and 27 percent.

12. The method of claim 1 or 2 wherein the liquid polyimide precursor compound has a viscosity of the order of between about 75 and 200 centipoise.

* * * * *



United States Patent [19]

Candelaria et al.

[11] **4,446,194**

[45] **May 1, 1984**

[54] **DUAL LAYER PASSIVATION**

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[73] Assignee: **Motorola, Inc.**, Schaumburg, Ill.

[21] Appl. No.: **391,047**

[22] Filed: **Jun. 21, 1982**

[51] **Int. Cl.**[3] **B05D 3/14**

[52] **U.S. Cl.** **428/428**; 357/54; 427/39; 427/93; 428/432

[58] **Field of Search** 427/38, 39, 93, 94, 427/96; 357/52, 53, 54; 428/428, 432

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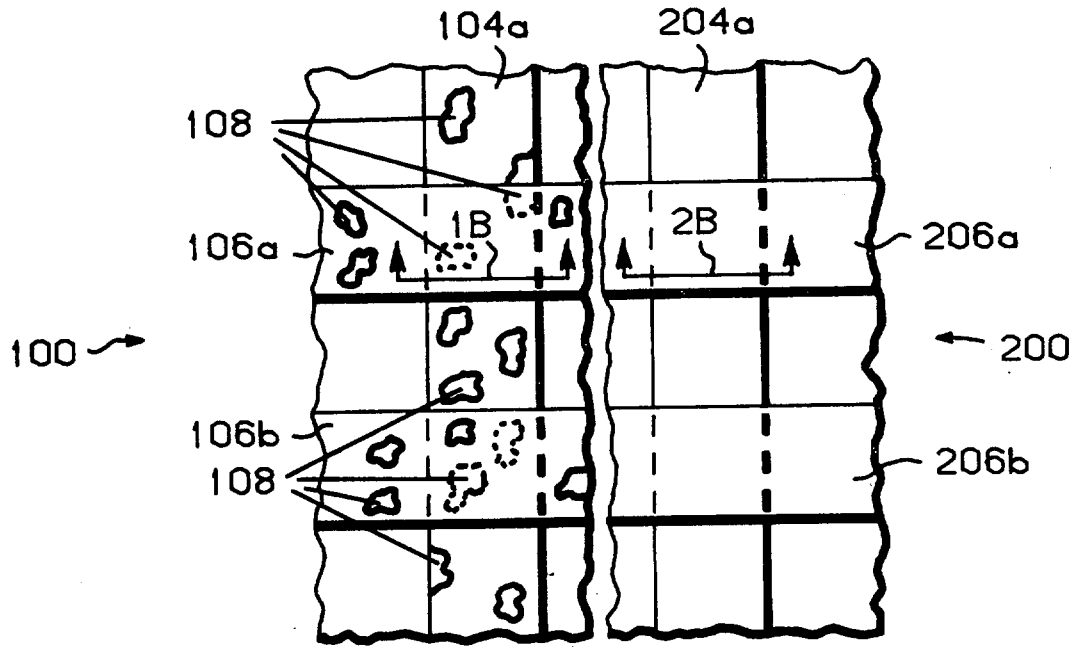
Attorney, Agent, or Firm—Robert M. Handy

[57] **ABSTRACT**

When multilayer-metal electronic devices are heated, voids can form in the metal layers. Void formation is avoided by using a double dielectric layer as the inter-layer dielectric. The double layer has a first oxide layer portion in contact with the first metal which is formed by plasma assisted chemical vapor deposition, and a second oxide layer portion formed by other means. The plasma formed oxide layer portion is believed to be in compressive stress relative to the substrate.

12 Claims, 4 Drawing Figures



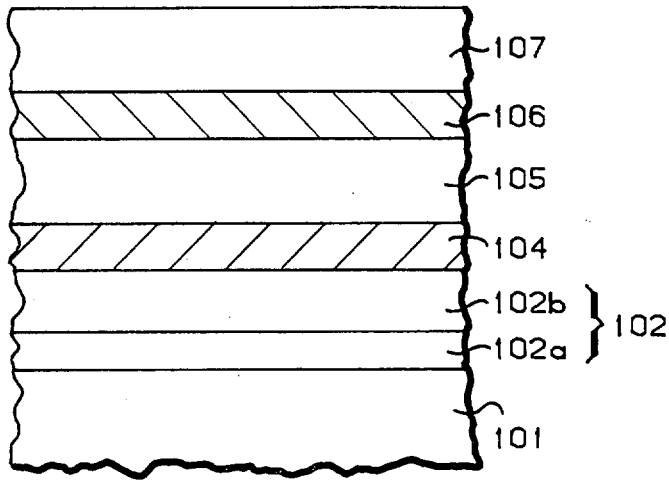


FIG 1B
- PRIOR ART -

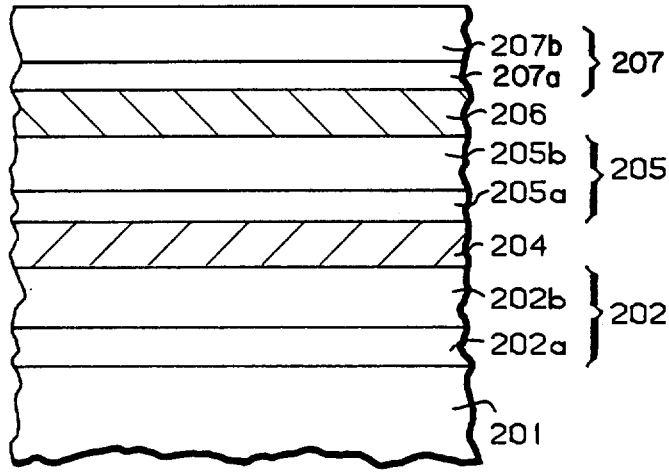


FIG 2B

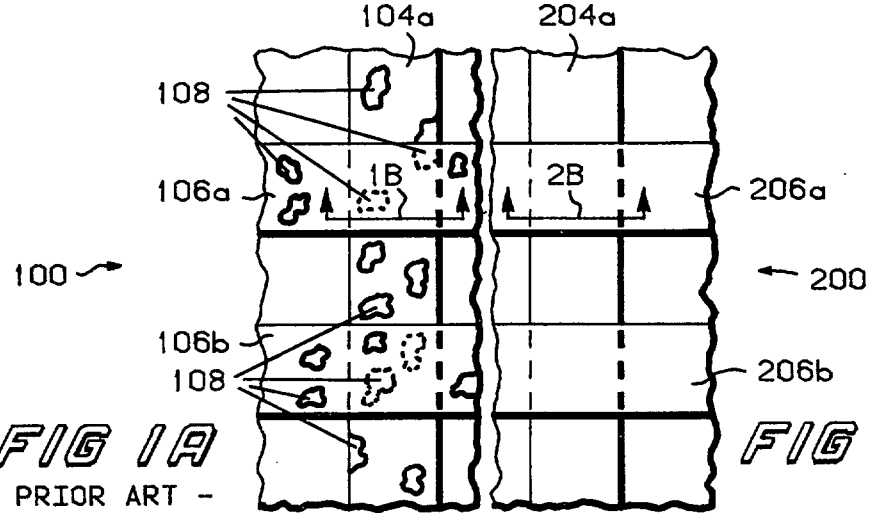


FIG 1A
- PRIOR ART -

FIG 2A

DUAL LAYER PASSIVATION

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates, in general, to means and methods for improved electronic devices, especially semiconductor devices and integrated circuits, and more particularly, to an improved manufacturing process for structures involving passivated metal layers or multiple passivated metal layers on nitride passivated substrates, and to structures, devices, and circuits made thereby.

2. Background Art

It is common practice in the manufacture of semiconductor devices and integrated circuits, and other electronic devices as well, to protect the semiconductor surface and the metal surface layers with a covering dielectric. This dielectric is referred to as the passivation layer or the metal passivation layer, and is often the outermost layer of the device. Openings are provided in the passivation layer through which external connections to the device may be made. As used herein, the word "device" is intended to include both individual devices, portions of devices, and collections of devices, as for example in integrated circuits and the like.

Frequently, a device will require multiple metal layers, one crossing over the other and separated by an interlayer dielectric. In this case the interlayer dielectric serves to passivate the first metal layer as well as insulate and separate it from the overlying second metal layer. Interlayer connection points are provided through openings formed for that purpose in the passivation layer serving as the interlayer dielectric.

With semiconductor and other devices having conductive substrates, a primary dielectric layer is also required between the substrate and any metal layers. This dielectric serves to passivate the substrate surface as well as insulate it from the metal layer or layers. Again, openings may be provided for connection points. When structures involving one or more metal layers superimposed on a dielectric layer and covered by a passivation layer are heated during subsequent manufacturing stages, as for example during assembly die bonding, it is found that voids frequently form in the metal layer or layers. These voids can be of appreciable size relative to the thickness and width of the metal conductor paths. The voids create weaknesses in the conductor paths which lead to reduced manufacturing yield and poorer reliability. This phenomenon is particularly severe when an aluminum alloy is used for the metal layer or layers and one of the several dielectric layers includes a nitride material. Thus, a need exists for a system of materials and manufacturing methods which reduces or eliminate the formation of voids in layered structures wherein one or more metal layers are sandwiched between dielectric layers. Because of their widespread use, there is a particular need for reducing or eliminating void formation in silicon oxide—nitride—aluminum alloy—doped oxide layer structures.

Accordingly, it is an object of this invention to provide an improved manufacturing method for the formation of metal—passivation layer structures wherein void formation in the metal layer is reduced or eliminated.

It is a further object of this invention to provide an improved manufacturing method for the formation of dielectric—first metal—first passivation—second metal—second passivation layer structures wherein

void formation in one or both metal layers is reduced or eliminated.

It is an additional object of this invention to provide an improved process for the manufacture of dielectric—metal—passivation layer structures and/or dielectric—first metal—first passivation layer—second metal—second passivation layer structure, wherein the passivation layer or layers comprise a double layer.

It is a further object of this invention to provide the double layer by means of a first layer portion of a plasma formed oxide in contact with the underlying metal, and a second layer portion of a doped oxide overlying the first layer portion.

It is an additional object of this invention to provide the first layer portion by means of plasma enhanced chemical vapor deposition.

It is an additional object of this invention to provide the double layer by means of a first layer portion of an oxide which is in compressive stress and a second layer portion of an oxide which is not in compressive stress.

It is a further object of this invention to provide improved electronic devices made by the methods of this invention.

SUMMARY OF THE INVENTION

In a first embodiment of the invention, a substrate is first coated with a primary passivation (dielectric) layer. It is desirable that this primary passivation layer have an outer surface comprising a nitride. A metal layer is next formed on the outer surface and then overcoated with a metal passivation layer comprising a first portion of a plasma formed oxide, and a second portion of a doped oxide formed by other means. Optional contacts between the substrate and the metal layer are provided by openings cut for that purpose in the primary passivation layer. The plasma formed oxide is conveniently created by plasma enhanced chemical vapor deposition.

In a second embodiment of the invention, a substrate is first coated with a primary passivation layer. A metal layer is next formed on the outer surface and then overcoated with a first metal passivation layer comprising a first portion of an oxide which is in compressive stress and a second portion of an oxide which is not in compressive stress. Optional contacts between the substrate and the metal layer are provided by openings cut for that purpose in the primary passivation layer.

In a third embodiment, a multilayer metal structure is obtained by taking the structure formed in the first or second embodiment and thereafter coating the first metal passivation layer with a second metal layer. It is desirable that the second metal be further coated with a second metal passivation layer of the same composition as the first metal passivation layer to inhibit void formation in the second metal layer. Optional contacts between metal layers are provided by openings cut for that purpose in the first metal layer passivation.

Devices made using the process are substantially more resistant to void formation in the metal layer or layers during heating of the devices, and have lower manufacturing cost and improved reliability.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1A is a top view of a portion of a prior art device having two layers of metal conductors, one crossing over the other, and showing voids formed in the metal layers.

FIG. 1B is a cross sectional view in simplified form of a crossover portion of the prior art device of FIG. 1A showing a typical arrangement of layers.

FIG. 2A is a top view of a portion of a device according to the present invention, having two layers of metal conductors, one crossing over the other and without voids.

FIG. 2B is a cross sectional view in simplified form of a crossover portion of the device of FIG. 2A showing the arrangement of layers.

DETAILED DESCRIPTION OF THE DRAWINGS

In the description which follows, the structure and materials are illustrated for the case of a silicon semiconductor substrate on which are formed various silicon oxide and nitride layers. It will be readily apparent to those of skill in the art that other substrate materials could be employed. As will be subsequently discussed, various other oxide and nitrides, as well as other dielectric materials, are believed to be useful.

FIGS. 1A–B show a portion of prior art device **100** comprising substrate **101**, covered by primary passivation layer **102** made up, for example, of buffer oxide layer **102***a* and nitride layer **102***b*. First metal layer **104** is formed on nitride layer **102***b* and overcoated by first passivation layer **105**. In single metal layer devices, first passivation layer **105** forms the outermost layer of the device and layers **106–107** are not present. In multilayer metal devices, first passivation layer **105** serves as the interlayer dielectric and is overcoated by second metal layer **106** and second passivation layer **107**. Methods for forming layers **102–107** are well known in the art. For example, passivation layers **105** and **107** are conveniently formed by chemical vapor deposition (CVD) of silicon oxide at temperatures in the range 350°–550° C., 450° C. being typical.

FIG. 1A illustrates the situation in which first metal layer **104** has been formed into vertical conductor **104***a*, and second metal layer **106** has been formed into two horizontal conductors **106***a–b*. Interconnections (not shown) between conductors **104***a* and **106***a–b* are optionally provided by means of openings ("vias") in first passivation layer **105** at the appropriate crossing points. Optional interconnections (not shown) between substrate **101** and conductors **104***a* and/or **106***a–b* are provided by means of other vias in layer **102** and **105** at desired locations. Methods for delineating conductor paths and forming vias are well known in the art.

FIG. 1A further illustrates the formation of voids **108** in conductors **104***a* and/or **106***a–b* as a result of heating the device (e.g. to temperatures above 450° C.) subsequent to the formation of metal layer **104** and passivation layer **105**, or alternatively, after the formation of metal layers **104** and **106** and passivation layers **105** and **107**. Voids **108**, shown pictorially in FIG. 1A, typically penetrate through the thickness of conductors **104***a* and/or **106***a–b*. They often occupy a substantial portion of the lateral cross-section of conductor **104***a*, conductors **106***a–b*, or both. Voids **108** can completely rupture conductors **104***a* and/or **106***a–b* causing the finished device to be inoperative. Even if the voids do not initially break conductors **104***a* and/or **106***a–b*, when the device is energized, the current density in conductor **104***a* and/or **106***a–b* is increased above the design value. This accelerates electro-migration effects which cause further enlargement of voids **108**, or growth of new voids, until conductors **104***a* and/or **106***a–b* are finally interrupted. Thus, not only will the initial manufacturing yield be lower, but those devices which may initially function will have reduced reliability and shorter useful lives.

FIG. 2A is a top view of device portion **200** according to the present invention, and FIG. 2B is a schematic cross sectional view of a crossover portion of the same device, showing the arrangement of layers. In FIG. 2A, first metal layer **204** has been formed into vertical conductor **204***a*, and second metal layer **206** has been formed into horizontal conductors **206***a–b*. As with the prior art device portion of FIGS. 1A–B, optional interconnections (not shown) between the metal layers and between the metal layers and the substrate can be provided by vias placed in passivation layers **205** and/or **202** at the appropriate locations. The lateral geometry of the conductor pathways in FIG. 2A is the same as in FIG. 1A, but there are no voids.

In FIG. 2B, substrate **201** is covered by primary passivation layer **202** comprising, typically, buffer oxide layer **202***a* and nitride layer **202***b*. Buffer oxide layer **202***a* is desirable when substrate **201** is a semiconductor such as silicon, but it is not necessary. Substrate **201** may be any suitable material, such as, ceramic, glass, semiconductor, metal, plastic, or a combination thereof, and may be single crystal, polycrystalline, amorphous or a combination thereof. It is desirable that the surface which receives the metal layers be reasonably smooth compared to the thickness of the metal layers.

First metal layer **204** is formed on nitride layer **202***b* and overcoated with first passivation layer **205**. In single metal layer devices, first passivation layer **205** forms the outermost layer of the device and layers **206–207** are not present. In multilayer metal devices, first passivation layer **205** serves as the interlayer dielectric and is overcoated by second metal layer **206** and second passivation layer **207**. Layer **207** passivates and protects layer **206** as well as the underlying layers exposed where portions of metal layer **206** have been removed in creating conductor paths **206***a–b*. Layer **207** is desirable but not mandatory.

It has been discovered that void formation associated with the prior art device structure of FIGS. 1A–B can be avoided by forming passivation layer **205** and desirably also layer **207** as double layers. The exact mechanism by which the use of a double layer inhibits void formation is not known. There is believed to be a large residual tensile stress present in metal layer **104**. The stress comes about as a result of the differential thermal contraction or expansion of the metal and dielectric layers which are formed at different temperatures. As additional layers are added on top of metal **104** (e.g. layer **105** and, optionally, layers **106** and **107**), the stress may be frozen in. It is believed that the doped or undoped oxides prepared by sputtering or chemical vapor deposition which are normally used as interlayer passivation dielectric **105** do not contribute to relieving this stress, so that when the devices are subsequently heated the residual stress accelerates void formation in the metal layer or layers.

Frequently, interlayer dielectric passivation **105** is prepared by chemical vapor deposition (CVD) of a substantially pure silicon oxide, or a silicon oxide doped with phosphorous, boron or other elements which assist in stabilizing the materials. Void formation is observed when aluminum or aluminum alloy metal layers are used in conjunction with these materials. It has been discovered that void formation in metal layer **104** is

inhibited by replacing passivation layer **105** with double layer **205**, in which first portion **205a** is formed by plasma assisted chemical vapor deposition (PACVD) and second portion **205b** is formed by other means, such as ordinary CVD. Similarly, void formation in layer **106** is inhibited by replacing passivation layer **107** with double layer **207** in a like manner.

The physical properties of the PACVD passivation material used for layer portion **205a** are believed to be different than the physical properties of the CVD passivation material used for layer **105** or layer portion **205b**. In "Plasma Deposition of Silicon Dioxide and Silicon Nitride", *Solid State Technology*, page 167, April 1981, by E. van de Ven, it is reported that PACVD SiO_2 shows intrinsic compressive stress on silicon, while conventional CVD SiO_2 shows intrinsic tensile stress. It is also known that addition of dopants such as phosphorus can reduce the intrinsic tensile stress of ordinary CVD oxides so as to produce doped oxide layers having little or no tensile stress relative to silicon substrate. It is not clear how these and other characteristics of the different passivation oxides interact with the metal layer to reduce void formation, but the different intrinsic stress characteristics are believed to be important, that is, void formation is reduced when layer portion **205a** is formed from a material having intrinsic compressive stress relative to the substrate when combined with layer portion **205b** which does not have intrinsic compressive stress relative to the substrate.

It is not practicable to use the PACVD oxide alone, that is, to make layer **205** entirely of PACVD oxide. This is because there are local variations in the etch rate which result in a loss of definition in the interconnect vias. Additionally, the etch rate and apparent porosity of the PACVD oxide is different depending on whether it rests on metal or nitride. The apparent porosity is greater over the nitride. Thus a via which extends beyond the edge of a metal stripe onto the nitride surface has very ragged edges over the nitride. Poor via definition reduces manufacturing yield. This problem is avoided by the double layer structure since definition of the vias is controlled by the relatively thicker outer CVD material, while the buffering or stress relief function to inhibit void formation in the underlying metal is provided by the comparatively thinner PACVD material placed in contact with the underlying metal layer.

The following example of a preferred structure and method of manufacture is illustrated for a silicon based semiconductor device having two metal layers. It will be readily apparent to one of skill in the art that the method and structure so described apply to a wide choice of substrate materials and device configurations, particularly those which utilize a nitride passivation layer or other dielectric materials underlying the metal layer which can produce a high stress condition in the metal.

Silicon wafer substrate **201** is preferably but not essentially, coated with thin buffer layer **202a** of silicon oxide of a thickness in the range of 10–200 nm, with 100 nm being convenient, and then coated with nitride layer **202b**, preferably of silicon nitride, of a thickness in the range 10–1000 nm, with 90–110 nm being convenient. First metal layer **204** of aluminum, or (96% Al):(4% Si) or (94% Al):(1.5% Si):(1.5% Cu) alloy is formed on layer **202b**. First metal layer **204** has a thickness in the range 20–2000 nm with 600–800 nm being convenient. Methods for forming metal layers of these and other materials are well known in the art. Sputtering was found to be convenient. Buffer oxide **202a** is typically thermally grown and nitride layer **202b** is typically deposited by vacuum CVD techniques. Such techniques are well known in the art. Other methods such as sputtering and PACVD are also useful.

Passivation layer **205** is formed as a double layer by depositing, in contact with metal layer **204**, first layer portion **205a** of a substantially pure PACVD silicon oxide of thickness in the range 10–500 nm, with 90–110 nm being convenient. Second layer portion **205b** is then deposited over first layer portion **205a**. Second layer portion **205b** comprises, typically, a 5% to 6.5% phosphorous doped CVD silicon oxide of thickness in the range 500–2000 nm, with 5.75% phosphorous and 810–990 nm thickness being preferred. While the thickness of layer portions **205a** and **205b** can be varied over a wide range, it is desirable that portion **205b** be thicker than portion **205a** in order to facilitate preparation of vias by chemical etching.

PACVD of silicon oxide for layer **205a** has been carried out in a commercial reactor, model 3000 PLASMA-II reactor manufactured by Applied Materials Corporation, 3050 Bowers Avenue, Santa Clara, Calif., using silane and nitrous oxide as source gases. Other silicon bearing gases and oxidant gases will also serve, and a wide range of source to oxidant ratios can be used so long as there is an excess of oxidant. Pressures in the range 100–500 microns (13.3–66.5 Pa), temperatures in the range 250°–500° C., silane flow rates in the range 6–600 ml per minute, silane to oxidant ratios in the range 1:2–1:100, and reactor power levels above 10 watts are useful. The deposition rate increases as power level and reactant flow rate are increased. A deposition rate of approximately 40 nm thickness per minute was obtained when the reactor was operated at a pressure of 250 microns (33.3 Pa), a power level of 150 watts, a silane flow rate of 60 ml per minute, a temperature of 300° C. and a silane to oxidant ratio of 1:15. These settings were found to be convenient. The index of refraction of PACVD silicon oxide layers was in the range 1.57–1.61, as compared to 1.45 for the phosphorous doped or substantially pure CVD silicon oxide layers. PACVD silicon oxide layers as used herein were found to be in compressive stress relative to [100] silicon substrates. Phosphorous doped CVD oxide layers as used herein, were found not to be in compressive stress relative to [100] silicon substrates.

The phosphorous doped CVD silicon oxide was prepared by methods well known in the art using a standard hot walled CVD reactor operating at temperatures in the range 350 to 550 degrees C., with 400 to 500 degrees C. being preferred and 450° C. being convenient. Conventional photoresist and etching steps were used, when desired, to open vias in layer **205** to permit contact to metal layer **204** and in layer **202** to permit connections between layer **204** and substrate **201**. In a single metal layer device, layer **205** serves as the final passivation layer and is typically the outermost layer of the device.

For a multilayer metal device, second metal layer **206** is formed on first passivation layer **205** which then serves as the interlayer dielectric. Metal layer **205** may be of any suitable material. The same materials and range of thicknesses as in first metal layer **204** are conveniently used for second metal layer **206**. Second metal passivation layer **207** is formed on second metal layer **206**. Layer **207** may be of the same or different dielectric materials as in layer **205**. It is convenient to use the

same materials and range of thicknesses, and to form layer **207** with the same double layer structure as in layer **205** in order to inhibit void formation in second metal layer **206**. In a two layer metal device, passivation layer **207** is often the outermost layer of the device. Openings (vias) are cut in layer **207** by means well known in the art to permit external connections to metal layer **206** and/or to permit interconnections between layers **206** and **204**. Sometimes, an organic coating is applied over layer **207** for further protection from the ambient.

Devices prepared according to the methods described above and without an organic overcoat were subjected to extended heating at temperatures exceeding 500° C. Prior art devices having similar layer thicknesses and prepared by substantially similar techniques, but using ordinary CVD oxides for passivation layers and lacking the double layer passivation structure of the present invention, were used as controls and similarly tested. The prior art devices showed significant void formation in the first and/or second metal layers while the devices prepared according to the present invention had no voids. The manufacturing yield and reliability of the devices prepared according to the present invention were thereby improved.

The invention has been illustrated for the situation wherein double layer portions **205***a*, **205***b* (and optionally **207***a*, **207***b*) were prepared by, respectively, PACVD of substantially pure silicon oxide, and CVD of phosphorous doped silicon oxide. It is believed that other preparation methods and materials will also serve, provided that the resulting films have properties similar to those obtained by these methods, in particular, that layer **205***a* exhibit intrinsic compressive stress and layer **205***b* not exhibit intrinsic compressive stress relative to substrate **201**. As used herein, the words "plasma derived" or "plasma assisted" refer to formation methods for dielectric passivation layers which use gas plasma and/or gas discharge reactions to form dielectric films, such as, but not limited to, plasma assisted chemical vapor deposition (PACVD).

The invention has further been illustrated for the situation where an aluminum alloy was used as the metallization. It will be readily apparent to those of skill in the art, that other metals can also be used. Accordingly it is intended to include these and other variations that are within the scope and spirit of the present invention.

We claim:

1. In a process for fabricating electronic devices wherein a first metal layer is formed on a first dielectric layer on a substrate, an interlayer dielectric is formed on said first metal layer, and a second metal layer is formed on said interlayer dielectric, the improvement comprising, forming said interlayer dielectric by depositing on said first metal layer a plasma derived oxide and overlying said plasma derived oxide with an other oxide formed by other means.

2. The process of claim **1** wherein said depositing step comprises depositing said plasma derived oxide by plasma enhanced chemical vapor deposition and wherein said other oxide is formed by chemical vapor deposition.

3. The process of claim **2** wherein said first dielectric layer comprises silicon nitride, said plasma derived oxide comprises silicon oxide, and said other oxide comprises a phosphorous doped silicon oxide.

4. In a process for fabricating electronic devices wherein a first metal layer is formed on a first dielectric layer on a substrate, an interlayer dielectric is formed on said first metal layer, and a second metal layer is formed on said interlayer dielectric, the improvement comprising, forming said interlayer dielectric by depositing on said first metal layer a first oxide exhibiting intrinsic compressive stress relative to said substrate, and covering said first layer by a second layer not exhibiting substantial intrinsic compressive stress relative to said substrate and formed by a different process than said first oxide layer.

5. The process of claim **4** wherein said depositing step comprises depositing said first oxide by plasma enhanced chemical vapor deposition.

6. The process of claim **5** wherein said first dielectric layer comprises silicon nitride, said first oxide comprises silicon oxide, and said second oxide comprises a phosphorous doped silicon oxide.

7. A process for fabricating electronic devices on a substrate comprising:

forming on said substrate a first dielectric layer;

forming on said first dielectric layer a first metal layer;

forming on said first metal layer a second dielectric layer having a predetermined compressive stress;

forming on said second dielectric layer a third dielectric layer substantially free of compressive stress; and

forming on said second dielectric layer a second metal layer.

8. The process of claim **7** wherein said first forming step comprises forming a first dielectric layer having an outer surface of silicon nitride, and said third forming step comprises forming said second dielectric layer by plasma assisted deposition of silicon oxide.

9. The process of claim **8** wherein said second forming step comprises forming said first metal from an aluminum alloy.

10. A process for fabricating electronic devices on a substrate comprising:

forming on said substrate a first dielectric layer;

forming on said first dielectric layer a first metal layer;

forming on said first metal layer a substantially pure oxide layer by plasma assisted chemical vapor deposition;

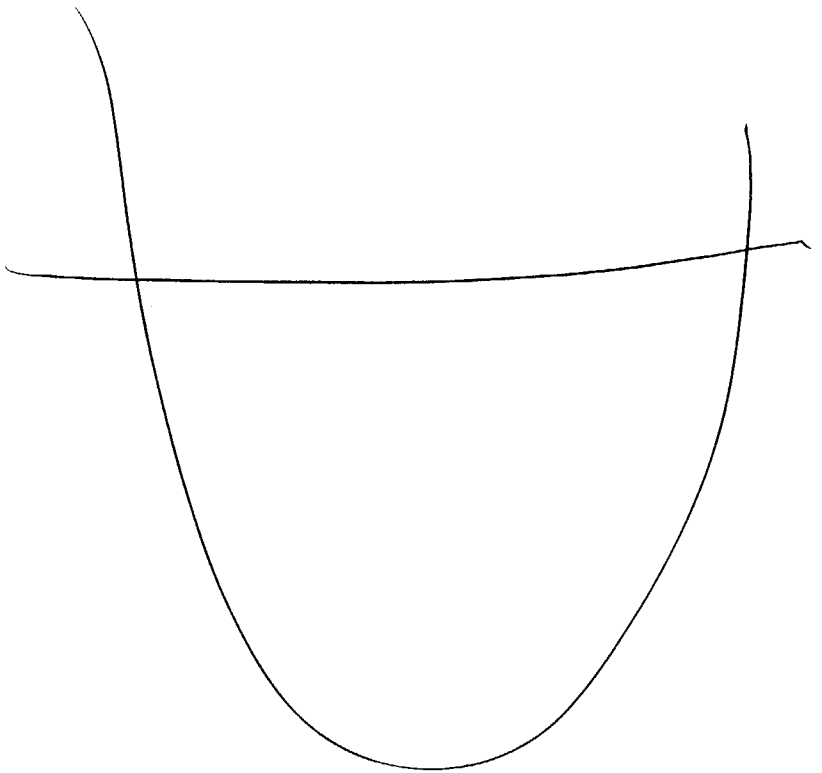
forming on said substantially pure oxide layer a doped oxide layer by chemical vapor deposition; and

forming on said doped oxide layer a second metal layer.

11. The process of claim **8** or **10** further comprising forming on said second metal layer a passivation layer comprising a first portion formed by plasma assisted deposition of silicon oxide and a second portion formed by chemical vapor deposition of silicon oxide.

12. An electronic device fabricated according to the process of claim **1**, **2**, **3**, **4**, **5**, **6**, **7**, **8**, **9**, or **10**.

* * * * *



United States Patent [19]

Goldman et al.

[11] **4,279,947**

[45] **Jul. 21, 1981**

[54] **DEPOSITION OF SILICON NITRIDE**

[75] Inventors: **Jon C. Goldman**, Tempe, Ariz.; **Larry D. McMillan**, Austin, Tex.; **James B. Price**, Phoenix, Ariz.

[73] Assignee: **Motorola, Inc.**, Schaumburg, Ill.

[21] Appl. No.: **23,568**

[22] Filed: **Mar. 26, 1979**

Related U.S. Application Data

[63] Continuation of Ser. No. 635,012, Nov. 25, 1975, abandoned.

[51] **Int. Cl.**[3] **C23C 11/14**

[52] **U.S. Cl.** **427/255.2**; 427/51; 427/94; 427/294

[58] **Field of Search** ..... 427/248 B, 94, 57, 294, 427/255.2

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Primary Examiner—Ronald H. Smith
Assistant Examiner—Janyce A. Bell
Attorney, Agent, or Firm—John A. Fisher

[57] **ABSTRACT**

Silicon nitride is pyrolytically deposited by the reaction of a halosilane with ammonia in an evacuated system. The process is particularly useful in providing uniform layers of silicon nitride on silicon wafers to be used in the fabrication of semiconductor devices.

4 Claims, 2 Drawing Figures

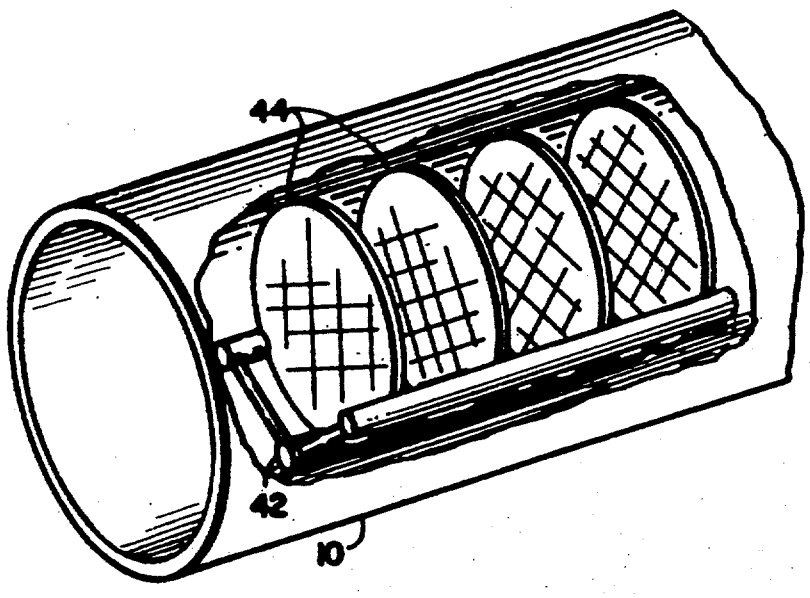


FIG. 1

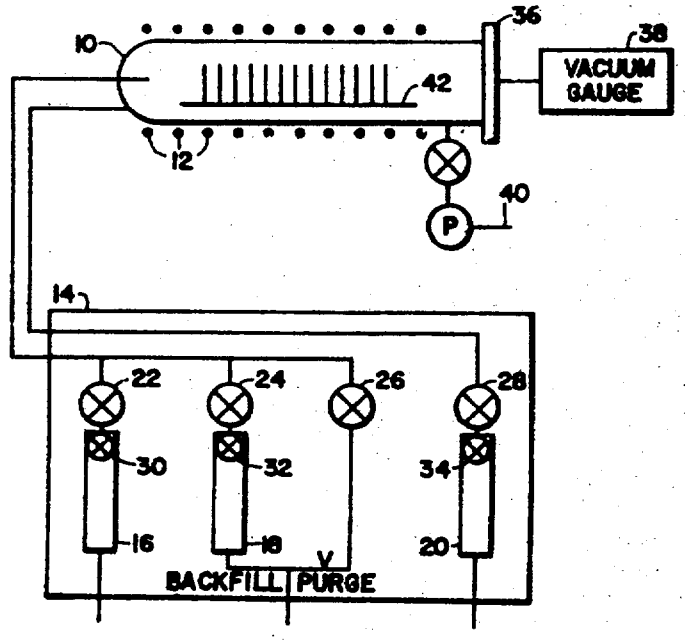
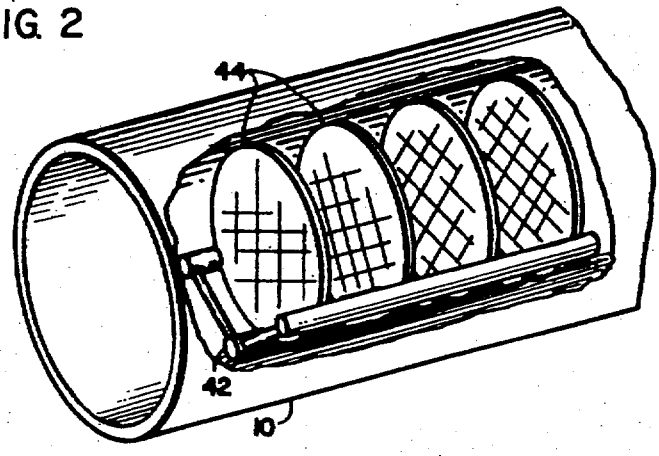

10
36
38
VACUUM GAUGE
42
12
40
P
14
22
24
26
28
30
32
34
16
18
20
BACKFILL
PURGE

FIG. 2


44
42
10

DEPOSITION OF SILICON NITRIDE

This is a continuation of application Ser. No. 635,012, filed Nov. 25, 1975, now abandoned.

BACKGROUND OF THE INVENTION

This invention relates to the pyrolytic deposition of silicon nitride onto a heated substrate and to substrates having uniform films of silicon nitride deposited thereon. More particularly, this invention relates to the deposition of silicon nitride by reacting a halosilane with ammonia in an evacuated system.

Silicon nitride (Si_3N_4) is a dense, chemically inert, dielectric material of extreme hardness, low thermal conductivity and high resistance to molecular diffusion. These properties have made silicon nitride an attractive and valuable material for a wide range of applications. For example, it is useful in the fabrication of semiconductor devices as oxidation masks, capacitor dielectrics for bit storage, masking layers, polish retarders, etc.

Various methods for depositing silicon nitride are known, but while the processes described in the prior art are functional in certain applications, they present drawbacks in other areas. For example, it has been found to be extremely difficult to deposit silicon nitride onto semiconductor substrates in a manner that will allow a good growth rate, uniform deposition, and a high quality coating in an economical process.

Thus, the deposition of silicon nitride by the reaction of either silane or dichlorosilane with ammonia at a pressure of about 1 atmosphere is conventional. However, the aforementioned processes are not completely satisfactory for depositing silicon nitride on semiconductor substrates because of the high cost of the equipment, over-all processing costs including the necessity of employing a carrier gas, and low throughput. Furthermore, these processes result in poor thickness uniformity on individual wafers and from wafer-to-wafer.

Accordingly, E. Tanikawa et al in "Chemical Vapor Deposition In An Evacuated System", C.V.D. 4th International Conference, ECS, G. F. Wakefield and J. M. Blocher, ed., 261–273 (1973) describe the reaction of silane and ammonia in an evacuated system to deposit silicon nitride on silicon wafers. However, wafers treated according to this process have been found to have a thicker ring of silicon nitride around the edge of the wafer together with silicon or silicon nitride dust and boat marks on the wafers. Furthermore, for best results, wafer size and spacing in the furnace must be uniform in carrying out the deposition.

It has now been found in accordance with this invention that silicon nitride can be deposited to provide surprisingly unexpected results by employing a halosilane as a reactant and carrying out the process in a vacuum.

SUMMARY OF THE INVENTION

It is an object of the invention to provide an improved method for the pyrolytic deposition of silicon nitride.

It is a further object of this invention to provide an economical process for the deposition of silicon nitride characterized by high through-put.

It is another object of this invention to provide uniform and continuous coatings of silicon nitride which are free from defects.

It is still another object of this invention to provide improved yields of semiconductor devices made from silicon wafers having silicon nitride deposited thereon.

In accordance with this invention, silicon nitride is pyrolytically deposited upon a substrate by contacting a mixture of a halosilane and ammonia with a substrate in a vacuum at an elevated temperature.

The process of this invention will be better understood by reference to the following description of the invention and the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic view of an apparatus for use in the process of this invention.

FIG. 2 is an isometric view, partly broken away, of a furnace tube loaded with wafers and suitable for use in the practice of this invention.

DETAILED DESCRIPTION OF THE INVENTION

Referring to the Figures, there is shown a furnace tube **10** heated by resistance heat coils **12** adjusted to give the desired temperature as described in detail below.

A gas panel generally referred to as **14** leads to the inlet end of furnace tube **10**. This gas panel contains a source of halosilane **16**, nitrogen **18** and ammonia **20**, which are admitted to the furnace tube by opening valves **22**, **24**, **26** and **28**. The halosilane is any monohalogenated or polyhalogenated silane, including the chlorosilanes, fluorosilanes, bromosilanes and iodosilanes. Preferably chlorosilanes such as chlorosilane, dichlorosilane, trichlorosilane and silicon tetrachloride are employed. The flow of gases is controlled by flow meter valves **30**, **32** and **34**. An end cap **36** is in engagement with furnace tube **10** to provide a vacuum seal within the tube, and the pressure is read by vacuum gauge **38**. Exhaust **40** serves to vent by-products and unreacted starting materials from the tube. As shown, the furnace tube holds a quartz boat **42** loaded with a plurality of silicon wafers **44**, which are positioned with their broad surfaces perpendicular to the cylindrical axis of the tube. The wafer positioning is clearer in FIG. 2. Preferably, a spacing of 50 to 500 mils between wafer surfaces is employed, with as many wafers as can be accommodated by the tube being processed at one time. While the type of wafer positioning shown in the drawings provides for maximum utilization of the tube, other means of positioning the wafers are contemplated. Furthermore, the process can be carried out in different types of vacuum apparatus.

In carrying out the process of this invention, the furnace tube is heated to the appropriate temperature for the particular halosilane and purged with nitrogen. Then the boat containing silicon wafers is loaded into the tube. The selected temperature should be high enough to give an acceptable growth rate while minimizing the competitive thermal decomposition of the halosilane to produce silicon. Generally a temperature between about 650° C. and 1000° C. is employed.

Another feature of this invention is that a temperature ramp can be established within the furnace tube. Thus, there can be a temperature variation along the tube, up to 100° C., and preferably from 10° C. to 50° C., with the lowest temperature being near the gas inlet end of the tube and the highest temperature near the opposite end of the tube. It has been found that utilizing a temperature ramp allows more flexibility in optimizing

down-the-boat uniformity and deposition rate. Higher temperatures increase both the deposition rate and the source gas depletion. Source gas depletion decreases wafer uniformity down the boat. Since higher deposition rates are desirable to increase throughput, one compensates for source gas depletion by temperature ramping, with the more depleted end at the highest temperature.

After the boat has been loaded into the tube and the desired temperature achieved, a vacuum less than 50μ is established. Then, ammonia and halosilane are admitted to the tube, bringing the pressure to from about 300 millitor to about 10 torr. The flow is regulated so that the mole ratio of ammonia to halosilane is from about 1 to 500:1. Furthermore, the ammonia is metered into the furnace tube at a rate between about 0.01 and 10 cc/sec, while the halosilane is metered into the tube at a rate between about 0.01 and about 0.5 cc/sec. It has been found that the growth of silicon nitride under these conditions is about 5 to 100 A°/minute; the process is continued until the desired thickness is deposited on the wafers. For most semiconductor applications, 200–2000 A° thick layers are desired, but the process of the invention is suitable to deposit layers of any thickness.

The silicon nitride layers produced according to this process have been found to have many advantages over those produced by prior art processes. Thus, the peripheral ring of thicker nitride found on wafers treated with silane and ammonia under vacuum is eliminated. Furthermore, silicon or silicon nitride dust formation and boats marks found in the aforementioned silane process were reduced to an insignificant level. Since the silicon nitride layers are uniform, more devices can be made from semiconductor wafers treated in accordance with this invention, further enhancing the attractiveness of the process.

The following example will serve to illustrate the practice of this invention.

EXAMPLE 1

One hundred fifteen precleaned 3-inch diameter silicon wafers were loaded into a three-rail quartz boat 16 inches long with 3/32 inch wafer spacing; in accordance with standard diffusion techniques, five dummy wafers were placed at each end of the boat. Then the boat was placed in a 101 mm outside diameter quartz tube in a thermco furnace. The temperature profile of the furnace was ramped so that thermocouple measurements at three equidistant points covering the center 20 inches of the furnace gave readings of 730° C., 750° C. and 770° C. respectively, with the lowest temperature at the end adjacent to the gas inlet. The furnace was evacuated to less than 50μ and purged with nitrogen for ten minutes at a pressure of 2 torr. Then the nitrogen was turned off and the system pumped down to a pressure less than 50μ. Ammonia was injected at a flow rate of 0.24 cc/sec for one minute. Then dichlorosilane was injected at a flow rate of 0.02 cc/sec while continuing the injection of ammonia. After 60 minutes, the dichlorosilane flow was terminated and the ammonia flow was terminated one minute later. These flow rates correspond to a molar ratio of ammonia to dichlorosilane of about 12 to 1. Then the furnace was pumped to a pressure of less than 50μ and purged with nitrogen for five minutes at a pressure of 2 torr. The vacuum valve was closed and the system back-filled with nitrogen. The boat was unloaded and the wafers evaluated. They were found to have a 1000A° thick layer of silicon nitride which was uniform from wafer to wafer ±10%, and around the wafer ±1%; the wafers exhibited no haziness and no boat marks.

What is claimed is:

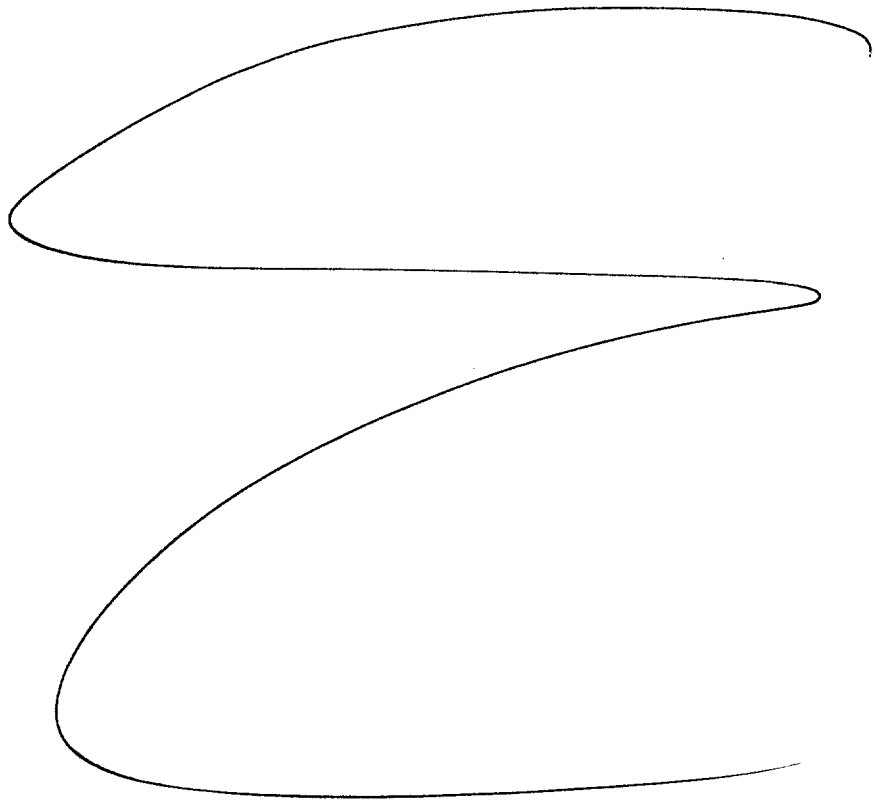
1. A method for the pyrolytic deposition of silicon nitride upon a plurality of substrates which comprises placing said plurality of substrates in a reactor tube with their broad faces perpendicular to the flow of a mixture of dichlorosilane and ammonia at a temperature of from about 650° C. to about 1000° C. in a vacuum of about 300 millitorr to about 10 Torr.

2. The method of claim 1 where said temperature is from about 770° C. to about 780° C.

3. The method of claim 1 wherein the temperature is ramped up to about 100° C. along the direction of said flow.

4. The method of claim 1 wherein the temperature is ramped up from 10° C. to 50° C. along the direction of said flow.

* * * * *



US005367494A

United States Patent [19]

Shebanow et al.

[11] Patent Number: 5,367,494

[45] Date of Patent: Nov. 22, 1994

[54] RANDOMLY ACCESSIBLE MEMORY HAVING TIME OVERLAPPING MEMORY ACCESSES

[75] Inventors: Michael C. Shebanow, Austin; Mitchell K. Alsup, Dripping Springs; Hunter L. Scales; George P. Hoekstra, both of Austin, all of Tex.

[73] Assignee: Motorola, Inc., Schaumburg, Ill.

[21] Appl. No.: 113,632

[22] Filed: Aug. 31, 1993

Related U.S. Application Data

[63] Continuation of Ser. No. 702,880, May 20, 1991, abandoned.

[51] Int. Cl.[5] G11C 8/00; G11C 7/00

[52] U.S. Cl. 365/230.03; 365/230.05; 365/230.06; 365/230.08; 365/189.04; 365/189.05; 365/193

[58] Field of Search 365/230.03, 230.05, 365/230.06, 230.08, 189.04, 189.05, 193

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Primary Examiner—Timothy P. Callahan

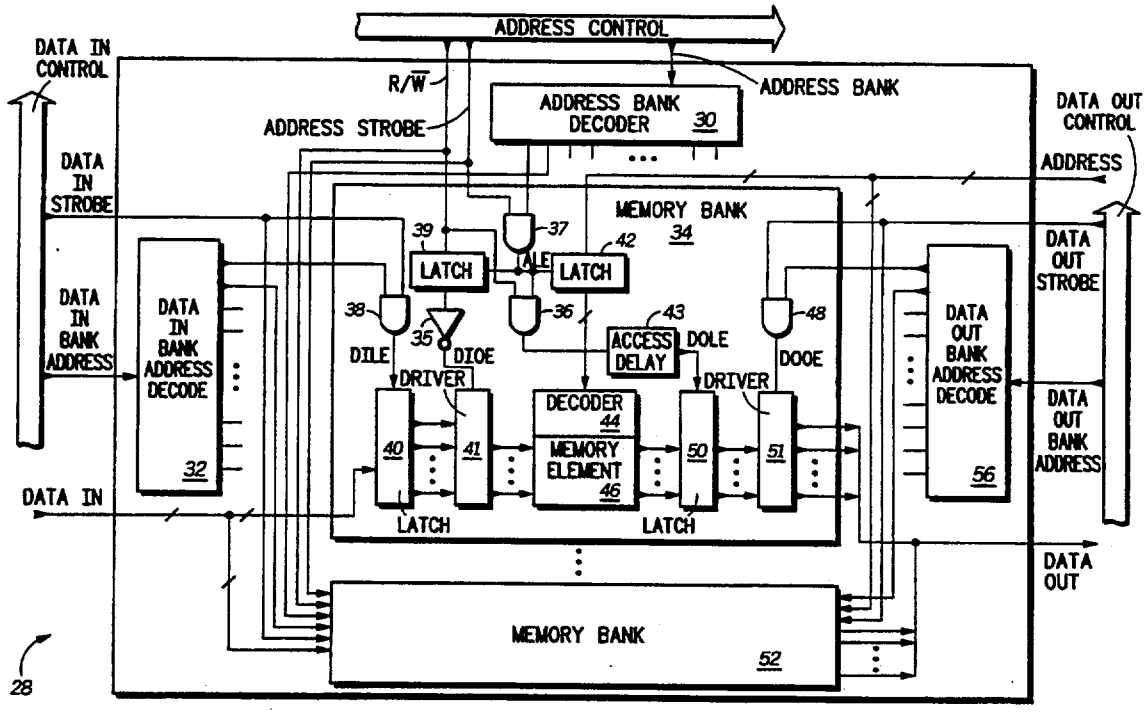
Assistant Examiner—Trong Phan

Attorney, Agent, or Firm—Elizabeth A. Apperley

[57] ABSTRACT

A memory device (28) executes memory access operations of two or more storage locations concurrently. The memory device (28) is comprised of a plurality of memory bank decode logic circuits (30, 32, 56) and a plurality of memory banks (34, 52). Each of the decode logic circuits decodes a first information and control signal set to enable a first memory bank to begin and complete a memory access operation. Each memory bank is comprised of a plurality of latch circuits (39,40, 42, 50) to store a predetermined information and control signal set necessary to perform the memory access operation. A second control signal and information set may, therefore, enable a second memory bank within the memory device (28) to perform a second memory access operation concurrently in time with the first memory access operation.

11 Claims, 4 Drawing Sheets



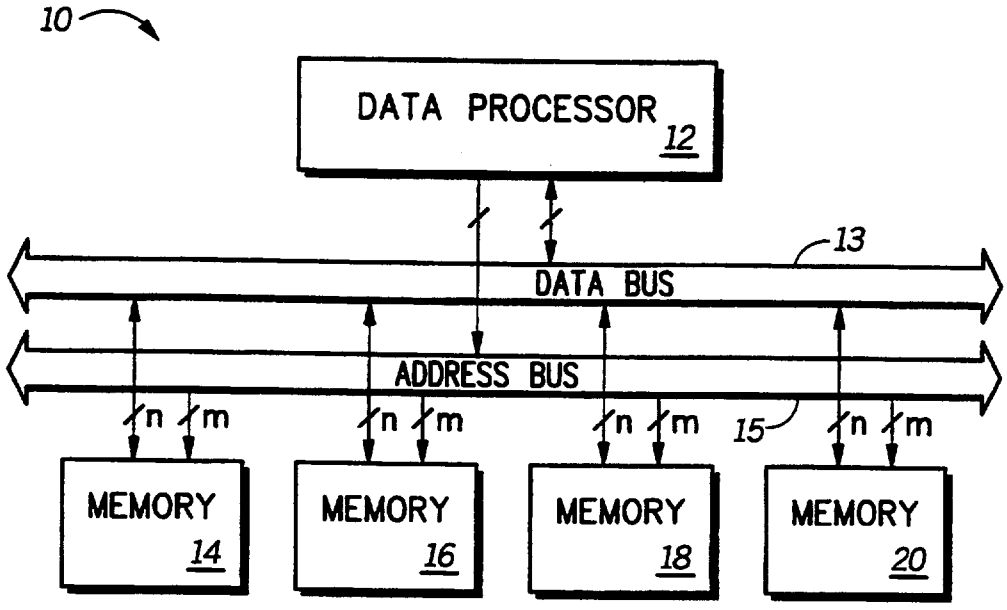


FIG.1(A)
-PRIOR ART-

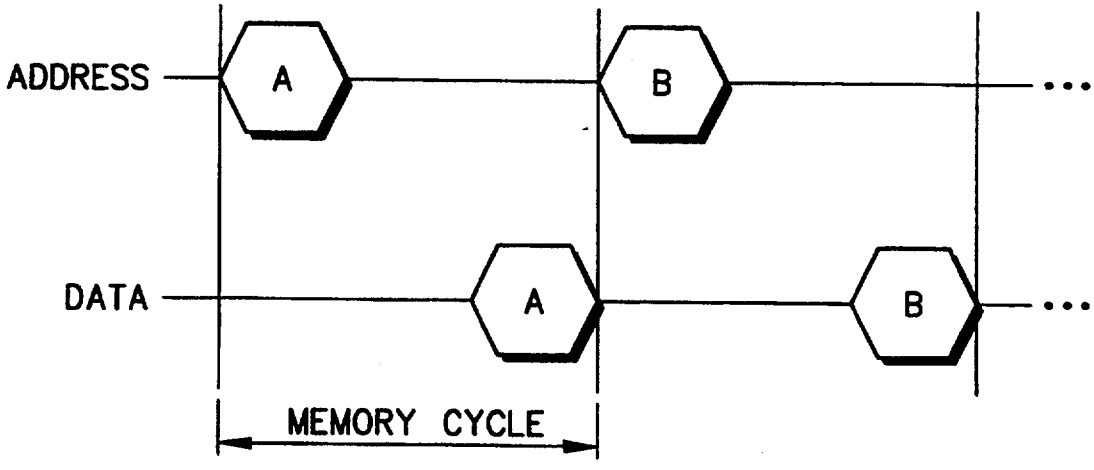


FIG.1(B)
-PRIOR ART-

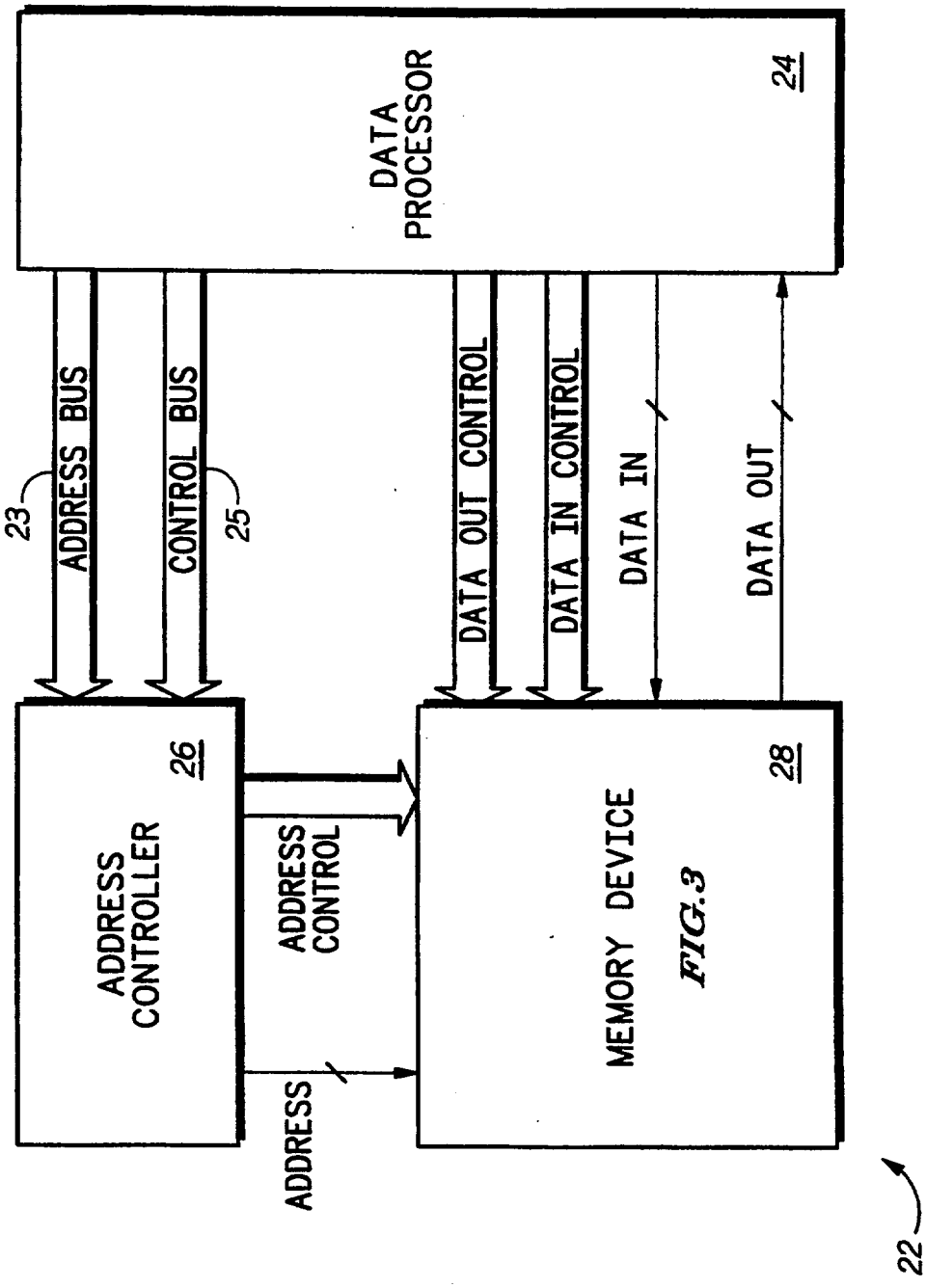

DATA PROCESSOR
24
ADDRESS BUS
23
CONTROL BUS
25
DATA OUT CONTROL
DATA IN CONTROL
DATA IN
DATA OUT
ADDRESS CONTROLLER
26
ADDRESS CONTROL
ADDRESS
MEMORY DEVICE
FIG.3
28
22

FIG.2

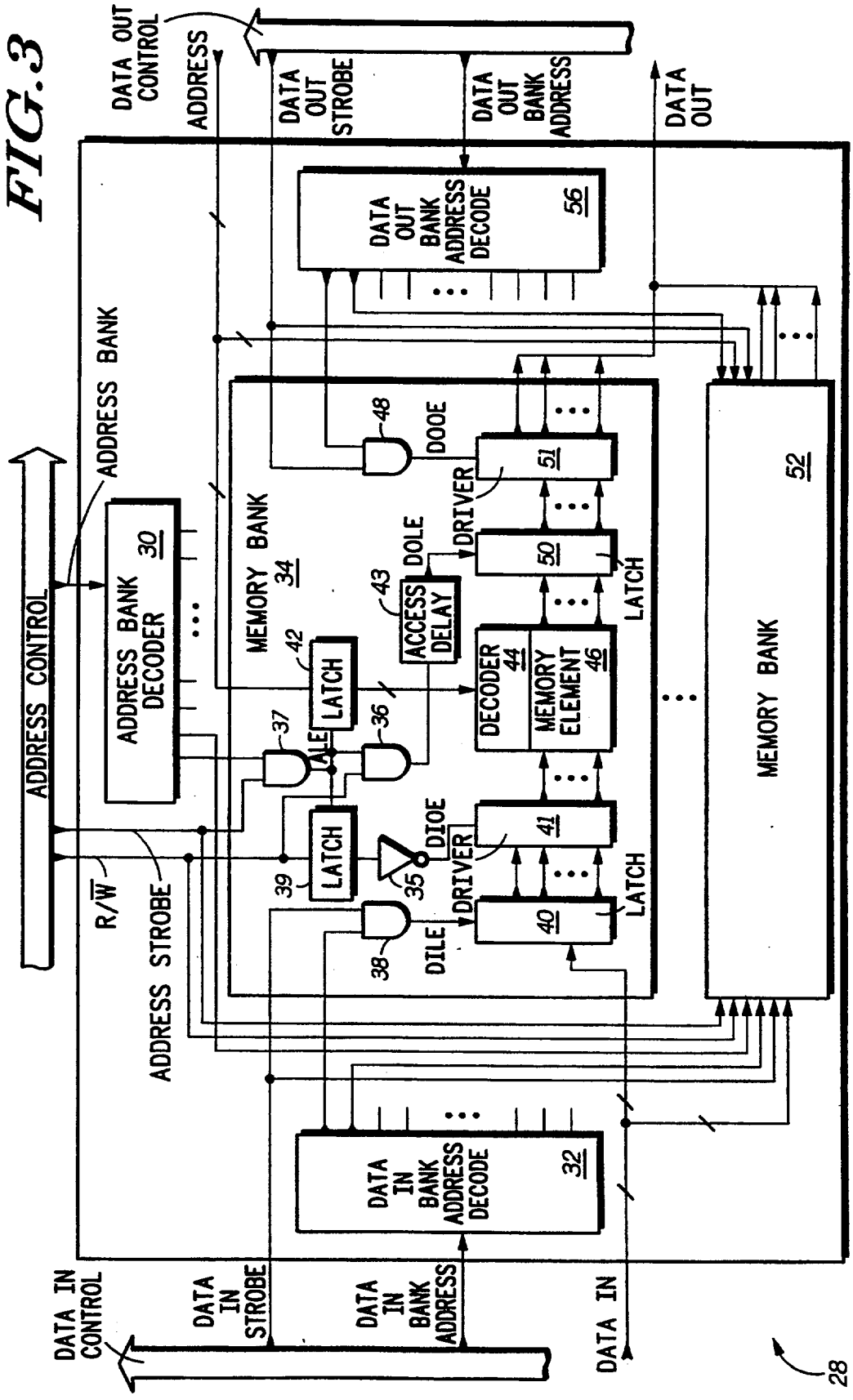


FIG. 3
DATA OUT CONTROL
ADDRESS
DATA OUT STROBE
DATA OUT BANK ADDRESS
DATA OUT
DATA OUT BANK ADDRESS DECODE
56
ADDRESS BANK
ADDRESS CONTROL
ADDRESS BANK DECODER
30
MEMORY BANK
34
48
DOOE
51
DRIVER
50
LATCH
DOLE
43
ACCESS DELAY
42
LATCH
DECODER
44
MEMORY ELEMENT
46
37
36
ALE
39
LATCH
35
DIOE
41
DRIVER
40
LATCH
38
DILE
R/W
ADDRESS STROBE
52
MEMORY BANK
DATA IN BANK ADDRESS DECODE
32
DATA IN CONTROL
DATA IN STROBE
DATA IN BANK ADDRESS
DATA IN
28

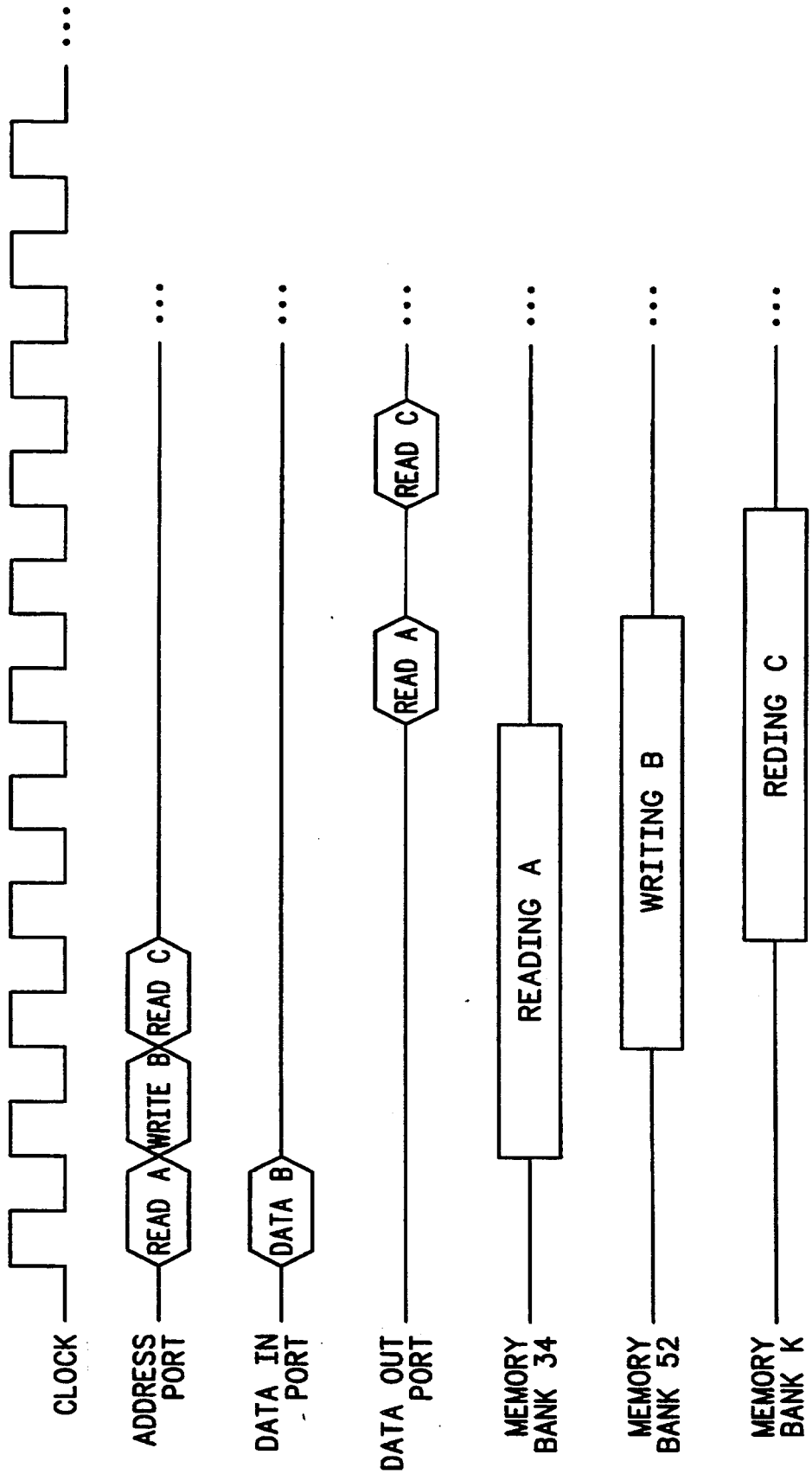

CLOCK
ADDRESS PORT
READ A
WRITE B
READ C
DATA IN PORT
DATA B
DATA OUT PORT
READ A
READ C
MEMORY BANK 34
READING A
MEMORY BANK 52
WRITING B
MEMORY BANK K
REDING C

FIG. 4

RANDOMLY ACCESSIBLE MEMORY HAVING TIME OVERLAPPING MEMORY ACCESSES

This application is a continuation of prior application Ser. No. 07/702,880, filed May 20, 1991, now abandoned.

FIELD OF THE INVENTION

This invention relates generally to memories and more particularly, to a randomly accessible memory.

BACKGROUND OF THE INVENTION

As data processing systems operate at faster speeds, associated peripheral memory devices must be able to function at compatible frequencies. However, as semiconductor technologies improve performance, the frequency at which a data processing system operates has increased to equal or even surpass the operating frequency of peripheral memory devices. In the latter case, the data processing system must often wait several clock cycles for information to be received from peripheral memory devices. Consequently, several techniques have been introduced to alleviate or shorten the latency between the performance of peripheral memory devices and the performance of the data processing system.

In one technique, a fast memory device called a "cache" is placed between the data processing system and a peripheral memory device. In this example, a peripheral memory device typically stores the bulk of information needed or provided by the data processing system. However, the peripheral memory device is not able to provide information in a single clock cycle and the data processing system must wait for several clock cycles before beginning to process another instruction. In comparison, the fast memory device provides information very quickly. Therefore, if the fast memory device is used to store the information values which are most often accessed by the data processing system, the period of time which the data processing system waits to receive information is generally shortened. By using this technique, the bulk of the information is still stored in the peripheral devices, but the information most frequently used is stored in the fast memory device.

The fast memory device may be integrated within the structure of the data processing system or implemented externally between the data processing system and the peripheral memory device. In either case, the fast memory device is an expensive solution. If the fast memory device is integrated within the structure of the data processing system as a portion of the semiconductor device, the fast memory device consumes a substantial amount of circuit area. Rather than providing other circuitry to further enhance the functionality of the data processing system, a fast memory device must be integrated in the data processing system to maintain the highest operating frequency. If one or more fast memory devices are implemented externally to the data processing system, the additional external fast memory devices result in a higher system overhead cost.

In a second technique, a memory subsystem compensates for the difference in the operation frequencies of the memory subsystem and the data processing system by allowing multiple concurrent accesses of different addresses. The multiple concurrent accesses are accomplished by providing a plurality of memory banks wherein each of the memory banks is independently and distinctly addressed and controlled. When the addresses

of the memory banks are arranged such that the consecutive addresses are provided by n different memory banks, where n is an integer, the memory subsystem is n-way interleaved.

When the data processing system accesses the peripheral memory devices in an interleaved manner, a first address of a first memory bank is accessed and then a first address of a second memory bank is concurrently accessed. Similarly, a plurality of other memory banks may be accessed while the first and the second memory banks continue to process a respective memory access. During an interleaved memory access, the data processing system may access any predetermined number of addresses concurrently.

When the data processing system provides an address to access one of a plurality of contiguous information values, the address is decoded and indicates which one of the plurality of memory banks contains the information value. To access the memory banks in an interleaved manner, addresses must be decoded such that the plurality of contiguous information values are contained in different memory banks and, therefore, may be accessed concurrently.

In a standard memory device, an access time is defined as the time from the start of execution of an operation to the end of operation execution. For example, in a read operation in the standard memory device, the access time is defined as the time from the start of execution of the read operation until the data read during the read operation is ready for use in a subsequent operation. The time from the start of execution of an operation until the device may execute another operation is referred to as the "cycle time."

In an interleaved memory access, the cycle time necessary to execute a first access of the first memory device is dependent on the cycle time of the first memory device. However, the time necessary to begin execution of subsequent operations is shortened, since the subsequent operations are executed concurrently with the first memory access. Although the cycle time of each of the peripheral memory devices remains the same, the data processing system is able to overlap the accesses of each of the peripheral memory devices and, therefore, increases the number of operations executed in a given amount of time.

Although interleaved addressing allows the data processing system to concurrently access peripheral memory devices, the overhead cost is expensive. For example, a predetermined number of external peripheral memory devices is necessary to implement interleaved addressing and, therefore, results in higher system overhead costs.

Both the fast memory device implementation and the interleaved addressing method result in an increased system overhead cost. Additionally, if the fast memory device is integrated within the structure of the data processing system, the designer of the data processing system must compromise between system functionality and system cost.

SUMMARY OF THE INVENTION

The previously mentioned needs are fulfilled with the present invention. Accordingly, there is provided, in one form, a randomly accessible memory having time overlapping memory accesses. The randomly accessible memory is comprised of a plurality of storage banks. Each storage bank is independently addressable and comprises an address port for receiving an input ad-

dress, a data port for communicating data, an array of memory storage elements, and a storage means coupled to the array of memory storage elements for storing address information, and either input data or output data in response to the input address. The storage banks are implemented in a single integrated circuit and a plurality of the storage banks are accessed during a plurality of multiple overlapping time periods.

These and other features, and advantages, will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1(A) illustrates in block diagram form a known data processing system having a plurality of randomly accessed memory portions;

FIG. 1(B) illustrates in timing diagram form a common timing diagram of a memory access in one embodiment of the data processing system of FIG. 1(A);

FIG. 2 illustrates in block diagram form a data processing system having a randomly accessible memory in accordance with the present invention;

FIG. 3 illustrates in partial block diagram form a Memory Device as shown in FIG. 2; and

FIG. 4 illustrates in timing diagram form a timing diagram of the system of FIG. 2.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

Illustrated in FIG. 1(A) is a known data processing system **10** having a plurality of randomly accessed memory portions. Memory portions which are randomly accessed allow a user of the system to access information based solely on address or data values, and not on sequential ordering. Any address or data value may be accessed regardless of the address or data values previously accessed.

The data processing system **10** is generally comprised of a Data Processor **12** and a plurality of randomly accessed memory portions, Memory **14**, Memory **16**, Memory **18**, and Memory **20**.

The Data Processor **12** provides information to and receives information from the plurality of randomly accessed memory portions via an Address Bus **15** and a Data Bus **13**, respectively. The Address Bus **15** is m bits wide and the Data Bus **13** is n bits wide, where both m and n are integers. If the Data Processor **12** requests a predetermined information value to be retrieved from the memories **14**, **16**, **18**, and **20**, an address signal corresponding to an associated storage location of the information value is transferred to the appropriate randomly accessed memory portion via Address Bus **15**. Assume in this example that Memory **14** contains the predetermined information value. Memory **14** then decodes the address signal to enable the associated storage location to provide the predetermined information value to the Data Processor **12** via the Data Bus **13**.

In general, a memory cycle reflects the length of time necessary to accomplish a read or write access of a memory portion in a data processing system. The time necessary to perform a memory access is determined by a cycle time of the memories **14**, **16**, **18**, and **20**.

A memory cycle of the data processing system **10** is illustrated in FIG. 1(B). In this example, a first information value is labelled "A" and a second information value is labelled "B." The information value A is accessed by transferring a first corresponding address value to a first predetermined one of the plurality of randomly accessed memories **14**, **16**, **18**, and **20** via the Address Bus **15**. The data processing system **10** must wait until the first predetermined memory portion decodes the corresponding address value to output the information value A via the Data Bus **13**. After the information value A is output, the information value B is accessed by transferring a second corresponding address value to a second predetermined one of the plurality of randomly accessed memories **14**, **16**, **18**, and **20** by the Address Bus **15**. The data processing system **10** must again wait until the second predetermined memory decodes the second corresponding address value to provide the information value B via the Data Bus **13**. When accessing both the information value A and the information value B, the memory cycle time is determined by the mount of time necessary to access and retrieve the information values from the corresponding memory portions.

If the cycle time of the plurality of the randomly accessed memories **14**, **16**, **18**, and **20** is slower than the operation frequency of the Data Processor **12**, the Data Processor **12** typically waits during a memory access. Generally, in a data processing system in which a data processor operates at a frequency which is substantially faster than the cycle time of an associated peripheral memory device, the productivity of the system is noticeably degraded. Assume that the Data Processor **12** operates at a frequency which is faster than the cycle time of the plurality of peripheral memory devices. During the period of time in which one of the plurality of peripheral memory device provides information, the Data Processor **12** typically waits without providing any other useful function. Therefore, even if the Data Processor **12** operates at a high frequency, the performance and efficiency of the entire data processing system is partially dependent on the cycle time of the peripheral memory devices. The performance and efficiency is also partially dependent on the number of peripheral memory devices which can concurrently perform memory access operations and the frequency with which information can be transferred between the peripheral memory devices and the data processing system.

The invention described herein provides a randomly accessible memory with time overlapping memory accesses which allows the data processing system to perform concurrent memory access operations in a fixed amount of time. The randomly accessible memory begins to process a new memory access operation at the start of each clock cycle. Therefore, more memory access operations are begun and subsequently completed in a shorter average amount of time. A plurality of other memory devices may be accessed while the first and the second devices process a respective first and a second memory access operation. During the memory access operations, the randomly accessible memory processes a plurality of memory access operations of one or all of the peripheral memory devices concurrently.

Illustrated in FIG. 2 is a data processing system **22** in accordance with the present invention which enhances and maximizes the efficiency with which memory access operations are performed. The data processing system **22** has a Data Processor **24**, an Address Controller **26**, and a Memory Device **28**.

The Data Processor **24** provides a plurality of address control and information signals necessary to perform a

memory access of the Memory Device 28. A multi-bit address information signal is transferred to an input of the Address Controller 26 via an Address Bus 23 and indicates the storage location of an information value in the Memory Device 28. The information value is stored in the Memory Device 28 in one of a plurality of memory banks.

The Data Processor 24 transfers the plurality of address control signals to a plurality of address control inputs of the Address Controller 26 via a Control Bus 25. The plurality of address control signals provides control information necessary to enable the Address Controller 26 to perform a memory access operation.

The Address Controller 26 is comprised of a conventional standard logic circuit (not shown) which provides address control and information signals to a plurality of address inputs of the Memory Device 28. The Address Controller 26 determines the address of a predetermined memory storage location and a corresponding one of a plurality of memory banks which is enabled during a read or write operation of the Memory Device 28. The Address Controller 26 provides a multi-bit signal labelled "Address" to indicate the address of the memory storage location of the predetermined information value requested by the Data Processor 24. The Address Controller 26 also provides a plurality of address control signals to enable one of a plurality of memory banks (not shown) via a bus labelled "Address Control". In the preferred embodiment, the Address Control bus is comprised of three signals respectively labelled "Address Strobe," "R/$\overline{W}$," and "Address Bank."

The Address Strobe signal enables the Memory Device 28 to provide a memory storage location for an information value. The R/$\overline{W}$ (Read/Write) signal provides control information to enable the Memory Device 28 to either read an information value from or write an information value to a predetermined memory storage location. The multi-bit Address Bank signal enables a predetermined one of the plurality of memory banks to participate in a memory access operation.

The Data Processor 24 also provides a plurality of data control and information signals necessary to either read an information value from or write an information value to a predetermined memory storage location. To obtain the information value read from the predetermined memory storage location, a first data control signal is transferred to a first data control input of the Memory Device 28 illustrated in further detail in FIG. 3. The first data control signal is labelled "Data Out Strobe" and is transferred via a bus labelled "Data Out Control" which is illustrated in FIG. 2. When the Data Out Strobe signal is a logic high value, the Memory Device 28 is enabled to output an information value to a multi-bit bus labelled "Data Out." A second data control input is labelled "Data Out Bank Address" and is also transferred by the Data Out Control bus. The Data Out Bank Address signal also enables a predetermined one of the memory banks to provide an information value to the Data Out bus.

To write (i.e. store) the information value to a predetermined memory storage location, a third data control signal is transferred from the Data Processor 24 to a third data control input of the Memory Device 28. The third data control signal is labelled "Data In Strobe" and is transferred via a bus labelled "Data In Control." The Data In Strobe signal enables the Memory Device 28 to latch an information value to be written to a predetermined memory storage location. A fourth data control signal is transferred from the Data Processor 24 to a fourth control input of the Memory Device 28. The fourth data control signal is labelled "Data In Bank Address" and is also transferred via the Data In Control bus. The Data In Bank Address signal enables a predetermined one of the plurality of memory banks to write an information value to a predetermined memory storage location. The information value to be stored in the Memory Device 28 is transferred from the Data Processor 24 to an input of Memory Device 28 via a multi-bit signal labelled "Data In."

Memory Device 28 maximizes the efficiency with which the data processing system 22 performs a memory access operation. As illustrated in FIG. 3, the Memory Device 28 is generally comprised of an Address Bank Decoder logic circuit 30, a Data In Bank Address Decode logic circuit 32, a Data Out Bank Address Decode logic circuit 56, and a plurality of K memory banks, such as memory bank 34 and memory bank 52, where K is an integer.

Each one of the plurality of memory banks is comprised of an inverter 35, an AND gate 36, an AND gate 37, an AND gate 38, a latch circuit 39, a latch circuit 40, a driver circuit 41, a latch circuit 42, an Access Delay circuit 43, a decoder 44, a memory element 46, an AND gate 48, a latch circuit 50, and a driver circuit 51. The memory element 46 is a sub-block of memory within the Memory Device 28.

An encoded Data In Bank Address signal provides a multi-bit input to the Data In Bank Address Decode logic circuit 32 to enable a predetermined one of the plurality of memory banks to store an information value.

If the first memory bank 34 is enabled, the Data In Bank Address Decoder logic circuit 32 provides a control signal to a first input of AND gate 38. The Data In Strobe signal provides a second input to the AND gate 38. The output of the second AND gate 38 is a signal labelled "DILE," where DILE is an abbreviation for Data In Latch Enable. The DILE signal provides a control input to latch circuit 40.

The Data Processor 24 provides the multi-bit Data In signal to an input of each one of the plurality of memory banks. In memory bank 34, the Data In signal is connected to latch circuit 40 and provides an information value which is subsequently stored in a predetermined memory storage location during a write operation. The output of latch circuit 40 is connected to the driver circuit 41. The driver circuit provides a plurality of input signals to the memory element 46. Information output from the memory element 46 is connected to latch circuit 50. The latch circuit 50 provides a plurality of information inputs to driver circuit 51. A plurality of output signals of driver circuit 51 is transferred to the Data Processor 24 via the Data Out signal.

The Address Controller 26 provides the multi-bit Address signal to an address input to of each one of the plurality of memory banks. In memory bank 34, the Address signal is connected a plurality of information inputs of latch circuit 42. The output signals of latch circuit 42 are connected to decoder 44. The decoder 44 decodes the address location to determine the appropriate memory storage location of a predetermined information value within the memory element 46.

The Address Controller 26 also provides the multi-bit Address Bank signal to a plurality of control inputs of the Address Bank Decode logic circuit 30. The Address

Bank Decoder logic circuit 30 provides a signal to enable a predetermined one of the plurality of memory banks in response to the encoded Address Bank signal.

If the signal enables the memory bank 34, the decoded Address Bank signal provides a first input to AND gate 37. The Address Strobe signal provides a second input to AND gate 37 and an output of AND gate 37 is a signal labelled "ALE," where ALE is an abbreviation for Address Latch Enable. The ALE signal provides a control signal to both latch circuit 39 and latch circuit 42, and a first input to AND gate 36.

The R/$\overline{W}$ signal provides a second input to AND gate 36 and an input to latch circuit 39. The R/$\overline{W}$ signal indicates whether the data processing system 22 is executing an operation to read an information value from or write an information value to a predetermined memory storage location in the Memory Device 28. An output of latch circuit 39 provides an input to inverter 35.

An output of inverter 35 is a signal labelled "DIOE." DIOE is an abbreviation for Data In Output Enable. The DIOE signal provides a control input to driver circuit 41.

An output of AND gate 36 provides a delay control signal to enable the Access Delay circuit 43. The delay control signal enables the Access Delay circuit 43 to wait a predetermined amount of time before providing a control signal labelled "DOLE" to a control input of latch circuit 50. The DOLE signal controls a transfer of an information value from memory element 46 to latch circuit 50.

The Data Out Bank Address Decode logic circuit 56 decodes each one of the Data Out Bank Address signals to enable a predetermined one of the plurality of memory banks. If the Data Out Bank Address Decode logic circuit 56 decodes the Data Out Bank Address signal to provide an input to memory bank 34, the decoded Data Out Bank Address signal provides a first input to AND gate 48.

The Data Out Strobe signal provides a second input to the AND gate 48 and an output of AND gate 48 provides a signal to enable driver circuit 51. When driver circuit 51 is enabled, an information value stored therein is transferred to the Data Processor 24 via the Data Out signal.

MEMORY READ OPERATION

When an information value is read from the Memory Device 28, the Data Processor 24 provides the plurality of address control and information signals to the Address Controller 26 and the plurality of data control and information signals to the Memory Device 28.

During a memory read operation, the Address Bank signal provides an encoded input signal to the Address Bank Decode logic circuit 30. The Address Bank Decoder logic circuit 30 decodes the Address Bank signal to enable a predetermined one of the plurality of memory banks. Assume in this example that the encoded Address Bank signal signifies that the information value to be read is stored in memory bank 34. Therefore, the Address Decoder logic circuit 30 provides a decoded Address Array signal with a high logic value to the first input of AND gate 37.

The Address Strobe signal provides a second input to AND gate 37 and is a logic high value to indicate that the Data Processor 24 is addressing a portion of the Memory Device 28. The output of AND gate 37, the ALE signal, is a logic high value to indicate that a memory access of memory bank 34 is implemented. The ALE signal is connected to the first input of AND gate 36 and a control input of both latch circuit 39 and latch circuit 42.

The Address Controller 26 provides an address of a predetermined memory storage location in the Memory Device 28 to the plurality of inputs of latch circuit 42 via the Address signal. The address of the predetermined memory storage location is temporarily stored in the latch circuit 42 when the ALE signal is asserted with a logic one value. The contents of latch circuit 42 subsequently provide inputs to decoder 44. Decoder 44 decodes the Address signal to enable a memory storage location in the memory element 46 which corresponds to the address location transferred via the Address signal.

The R/$\overline{W}$ signal provides an input to latch circuit 39. The R/$\overline{W}$ signal indicates whether the data processing system 22 is executing an operation to read an information value from or write an information value to a predetermined memory storage location in the Memory Device 28. During a read operation of a memory storage location, the R/$\overline{W}$ signal provides a logic high value to both latch circuit 39 and the second input of AND gate 36.

Because the ALE signal is a logic high value during a memory access operation, latch circuit 39 is enabled to store the value of the R/$\overline{W}$ signal. The latch circuit 39 subsequently provides the value of the R/$\overline{W}$ signal to the input of inverter 35.

Therefore, the output of inverter 35, the DIOE signal, is a logic low value. Consequently, driver circuit 41 is not enabled to transfer an information value to the memory element 46.

The R/$\overline{W}$ signal also provides a logic high value to the second input of AND gate 36. As previously described, the ALE signal provides a logic high value to the first input of AND gate 36. Subsequently,the AND gate 36 provides a logic high value as a control input to the Access Delay circuit 43. When the output of AND gate 36 has a logic high value, the Access Delay circuit 43 is enabled to wait for a predetermined amount of time and then to provide the DOLE signal to enable latch circuit 50 in the illustrated form. The predetermined amount of time corresponds to the amount of time necessary for the memory element 46 to output an information value.

Therefore, during a read operation, the output of AND gate 36 has a logic high value and subsequently enables the Access Delay circuit 43 to provide the DOLE signal. When the DOLE signal has a logic high value, the latch circuit 50 is enabled to temporarily store an information value from the predetermined memory storage location in the memory element 46. The contents of latch circuit 50 are subsequently transferred to a plurality of inputs of driver circuit 51.

Additionally, when the information value is transferred from the Memory Device 28, the Data Processor 24 provides the plurality of data control and information signals to the Memory Device 28 to control the transfer of the information value. The data control signals are comprised of the Data In Strobe, the Data In Bank Address, the Data Out Strobe and the Data Out Bank Address signals.

The Data In Strobe signal provides the first input to AND gate 38 and is a logic low value to indicate that the Data Processor 24 is reading, and not writing, a portion of the Memory Device 28. As well, when the

information value is being read from, and not written to the Memory Device 28, the Data In Bank Address signal is not asserted. Therefore, the decoded Data In Bank Address signal provides a logic low value to the second input of AND gate 38.

Because both the Data In Strobe and the decoded Data In Array signals are a logic low value, the output of AND gate 38, the DILE signal, is also a logic low value. Thus, the DILE signal is not asserted and an information value is not transferred to the latch circuit 40.

The Data Out Strobe signal provides the first input to AND gate 48 and is a logic high value to indicate that the Data Processor 24 is performing a read operation of the Memory Device 28.

The Data Out Bank Address signal provides an input to the Data Out Bank Address Decode logic circuit 56. The Data Out Bank Address Decode logic circuit 56 decodes the Data Out Bank Address signal to identify a predetermined one of the plurality of memory banks which should be accessed. In this case, the encoded Data Out Bank Address signal signifies that the information value to be read is stored in memory bank 34. Therefore, the Data Out Bank Address Decode logic circuit 56 provides a decoded Data Out Bank Address signal with a logic high value to the second input of AND gate 48.

Because both the Data Out Strobe and the decoded Data Out Bank Address signals have a logic high value, the output of AND gate 48, the DOOE signal, is a logic high value. Driver circuit 51 is, therefore, enabled to provide the information value transferred therein by the latch circuit 50 to the Data Processor 28. The information value is transferred to the Data Processor 28 via the Data Out signal.

MEMORY WRITE OPERATION

Similarly, when an information value is transferred to and subsequently written to memory bank 34 of the Memory Device 28, the Data Processor 24 provides the plurality of address control and information signals to the Address Controller 26 and the plurality of data control and information signals to the Memory Device 28.

During the write operation to a predetermined memory storage location, the Address Bank signal provides an input signal to the Address Bank Decode logic circuit 30. The input signal subsequently provides a decoded Address Bank signal to identify one of the plurality of memory banks which should be accessed. Assume in this case, that the encoded Address Bank signal indicates the information value to be read is stored in memory bank 34. The Address Bank Decode logic circuit 30 then provides a decoded Address Bank signal with a logic high value to the first input of AND gate 37.

The Address Strobe provides a second input to AND gate 37 and is a logic high value to indicate that Data Processor 24 is accessing the Memory Device 28. Because both inputs to AND gate 37 have a logic high value, the output of AND gate 37, the ALE signal, also has a logic high value. The ALE signal provides the first input to AND gate 36 and a control input to both latch circuit 39 and latch circuit 42.

The Address signal transfers an address of a predetermined memory storage location to the latch circuit 42. Again, the address of the memory storage location is transferred to and temporarily stored in the latch circuit 42 when the ALE signal is a logic high value.

During an operation in which an information value is written to the memory element 46, the $R/\overline{W}$ signal has a logic low value. Because the ALE signal is a logic high value during a memory access operation, the latch circuit 39 is enabled to store the value of the $R/\overline{W}$ signal. The latch circuit 39 subsequently provides the value of the $R/\overline{W}$ signal to the input of inverter 35. The output of inverter 35, the DIOE signal, has a high logic value and provides a control input to driver circuit 41. Because the DIOE signal is a logic high value, the driver circuit 41 is enabled to transfer an information value stored therein to the memory element 46.

The $R/\overline{W}$ signal also provides a logic low value as the second input of AND gate 36. The AND gate 36 subsequently provides a logic zero value as a control input to the Access Delay circuit 43. Therefore, the Access Delay circuit 43 is not enabled to provide the DOLE signal to enable latch circuit 50 after a predetermined amount of time during a write operation.

The information value to be written to the memory element 46 is transferred to the latch circuit 40 via the Data In signal. Data control signals which are comprised of the Data Out Strobe, the Data Out Bank Address, the Data In Strobe and the Data In Bank Address signals enable the memory bank 34 to write the information value to the memory element 46.

The Data Out Strobe provides the first input to the AND gate 48 and is a logic low value to indicate that the Data Processor 24 is writing an information value to the Memory Device 28. Since the information value is written to the Memory Device 28, the Data Out Bank Address signal is not asserted. Therefore, the decoded Data Out Bank Address signal is not asserted and a logic low value is provided as the second input to AND gate 48. The output of AND gate 48, the DOOE signal, is then a logic low value and driver circuit 51 is not enabled to provide an output signal to Data Processor 24.

The Data In Strobe signal provides the first input to AND gate 38 and is a logic high value to indicate that the Data Processor 24 is writing a portion of Memory Device 28.

The Data In Bank Address signal provides an input to the Data In Bank Address Decode logic circuit 32. The Data In Bank Address Decode logic circuit 32 subsequently provides a decoded Data In Array signal to identify a predetermined one of the plurality of memory banks which should be accessed. In this case the encoded Data In Bank Address signal signifies that the information value to be written is stored in memory bank 34. Therefore, the Data In Bank Address Decode logic circuit 32 provides a decoded Data In Bank Address signal with a high logic value to the second input of AND gate 38.

Consequently, the output of AND gate 38, the DILE signal, has a high logic value and latch circuit 40 is enabled to store an information value to be written to the memory element 46. Likewise, because the output of AND gate 36 is a logic high value, the driver circuit 41 is enabled to write the information value stored in latch circuit 40 to the Memory element 46.

Latch circuit 40 stores and driver circuit 41 subsequently transfers the information value to the corresponding storage location in memory element 46 when the DILE and the DIOE signals are respectively a logic high value. The information value stored in latch circuit 40 is then written by the driver circuit 41 to the address

location in memory element 46 determined by the data processing system 22.

TIMING EXAMPLE

A timing example of the data processing system 22 is illustrated in FIG. 4. Assume that the user of the data processing system 22 executes a first instruction which reads an information value labelled "A" from the Memory Device 28. The information value A is stored in the memory bank 34. A second instruction is executed by the data processing system 22 writes an information value labelled "B" to the Memory Device 28. The information value B is stored in the memory bank 52. The data processing system 22 may then continue to execute a plurality of instructions to perform a respective plurality of memory access functions. For example, the data processing system 22 may request that an information value labelled "C" be read from Memory Device 28. In the known data processing system 10, the system must wait for the information value A to be accessed and retrieved from a first one of the plurality of randomly accessible memory portions before the information value B is accessed from a second one of the plurality of the randomly accessible memory portions. In the implementation of the data processing system 22, however, the system begins execution of the instruction to write the information value B immediately after beginning execution of the instruction to read the information value A as a result of the independent control and subsequent overlapped timing of the array of memory banks.

Assume that the clock signal illustrated in FIG. 4 represents the operating frequency of the Data Processor 24 in the data processing system 22. When the data processing system 22 reads an information value A, an instruction is executed to provide the appropriate information and control signals. The appropriate information and control signals are entered through an Address Port. Therefore, on a first clock cycle, the information and control signals associated with the read operation of information A are provided. On a second clock cycle, the Memory Device 28 begins to manipulate the information and control signals to execute the read operation in memory bank 34. The first step in the manipulation of the information and control signals is to write each pertinent signal value in the plurality of latch circuits 40, 42, and 50, illustrated in FIG. 3. The conductors used to transfer the control and information signals are then free to transfer another set of information and control signals associated with a different memory access operation.

After a predetermined number of clock cycles, the manipulation of the information and control signals necessary to read the information value A is fully executed, and the information value A is available to the Data Out Port.

While the read operation of information value A is being executed, a write operation of information value B to memory bank 52 is executed concurrently. During the first clock cycle, the information and control signals associated with reading information value A are provided by the Address Port and the system 22 also provides the information value B to a Data In Port. On the second clock cycle, when the Memory Device 28 begins to manipulate the information and control signals associated with the read operation of information value A, the data processing system 22 provides the information and control signals associated with the write operation of information value B to the Address Port. On a third clock cycle, the system 22 begins to manipulate the information and control signals necessary to execute the write operation in the memory bank 52. Again, the first step in the manipulation of the information is to store the pertinent signal values in the plurality of latch circuits (not shown) associated with the memory bank 52.

While information value A is being read and information value B is being written, an operation to read information value C from a memory bank (not shown) is executed concurrently. When the data processing system 22 reads an information value C, an instruction is implemented to provide the appropriate information and control signals via the Address Port. Therefore, on the third clock cycle, the information and control signals associated with the read operation of information C are provided to the Address Port. On a fourth clock cycle, the Memory Device 28 begins to manipulate the information and control signals to execute the read operation in the memory bank (not shown). The first step in the manipulation of the information and control signals is to write each pertinent signal value in the plurality of latch circuits 40, 42, and 50, illustrated in FIG. 3. Again, the conductors used to transfer the control and information signals are then free to transfer another set of information and control signals associated with a different memory access operation.

After a predetermined number of clock cycles, the manipulation of the information and control signals necessary to read the information value C is fully executed, and the information value C is available to the Data Out Port.

By utilizing the plurality of latch circuits such as 40, 42, and 50, associated with each one of the plurality of memory banks, several read or write operations of different memory arrays comprising the same memory device may be concurrently processed by the data processing system 22. The plurality of latch circuits effectively stores the information necessary to complete memory access operations in each one of the plurality of memory banks concurrently, thereby allowing each one of the plurality of memory banks to function independently of other memory banks. Therefore, a plurality of conductors connected between the Data Processor 24, the Address Controller 26 and the Memory Device 28 transfer signals associated with a current memory operation before a previous memory operation is fully executed.

The randomly accessible memory with time overlapping memory accesses allows the data processing system 22 to perform more memory access operations in a fixed amount of time. Because the Memory Device 28 may start to process a new memory access operation at the start of each clock cycle, more memory access operations are begun and subsequently completed in a fixed amount of time. As previously discussed, when a data processing system accesses a plurality of peripheral memory devices in an interleaved manner, a first address of a first peripheral memory device is accessed and then a first address of a second peripheral memory device is concurrently accessed. Similarly, a plurality of other memory devices may be accessed while the first and the second devices process a respective first and a second memory access operation. During the memory access operations, the randomly accessible memory processes a plurality of memory access operations of one or all of the peripheral memory devices concurrently.

In the data processing system 22, the Memory Device 28 is especially useful when implementing an interleaved memory access. The plurality of latch circuits, 40, 42, and 50, provide a means to store data and address information values of a first memory access. As the first memory access is being executed, the plurality of Address, Address Control, Data Out Control, Data Out, Data In Control, and Data In signals are free to begin execution of a second memory access. In the data processing system 22, a plurality of memory accesses may be executed concurrently. The address decode operation necessary to execute a plurality of interleaved memory accesses is controlled by the Address Controller 26.

There has been provided herein, a data processing system having a randomly accessible memory with time overlapping memory accesses. The randomly accessible memory is comprised of a plurality of memory arrays each of which has a plurality of latch circuits to store a first information value associated with a memory operation. Therefore, after the first information and control signals associated with a first memory operation are stored in the appropriate plurality of latch circuits, the conductors transfer a second information signal associated with a second memory operation. While one memory access operation is initiated in the Data Processor 24, one or more memory access operations may also be concurrently executed in the Memory Device 28.

It should be well understood that the randomly accessible memory with time overlapping memory accesses described herein provides an effective and unique solution to shorten the latency between the performance of peripheral memory devices and the performance of data processing system. By enabling the memory device associated with the data processing system to execute memory operations concurrently, the efficiency of the data processing system is noticeably improved. The circuitry used to enable the memory device to execute memory access operations concurrently does not occupy a large amount of circuit area, and is, therefore, relatively inexpensive to implement on a semiconductor device.

By now it should be apparent that there has been provided a data processor with a randomly accessible memory having time overlapping memory accesses. The implementation of the invention described herein is provided by way of example only. Many other implementations may exist for executing the function described herein. For example, in the data processing system 22, both the Data Processor 24 and the Address Controller 26 could be implemented using a variety of standard logic circuitry.

Additionally, the configuration of the Memory Device 28 might be modified in many ways. For example, the Address Bank Decode logic circuit 30, the Data In Bank Address Decode logic circuit 32, and the Data Out Bank Address Decode logic circuit 56 could be implemented in any form of standard logic circuitry which provides a decoding function. Any number of memory banks, such as 34 and 52, may comprise the Memory Device 28. The function described herein would continue to operate adequately with a plurality of memory banks, but the cost effectiveness of the number of memory banks must be determined by the user of the system. The described invention might also be modified by the manner in which the plurality of latch circuits is implemented. Again, numerous standard logic implementations might be used. As well, the random logic circuitry, such as AND gate 36, AND gate 37, AND gate 38, and AND gate 48, might be implemented as another form or logic gate. Likewise the decoder 44 functions to decode information values and may be implemented in a manner determined to be most efficient by the user of the data processing system 22. The memory element 46 may be implemented as any memory device. For example, the memory element 46 may be implemented as either a ROM (Read Only Memory), a RAM (Random Access Memory) or a DRAM (Dynamic RAM).

The memory device described herein provides a versatile and efficient circuit and method to implement a randomly accessible memory which execute memory operations concurrently. The memory device may be implemented in a variety of logic circuits as determined by a designer of a data processing system. The memory device will, however, increase the performance and efficiency of any system in which it is implemented.

While there have been described herein the principles of the invention, it is to be clearly understood to those skilled in the art that this description is made only by way of example and not as a limitation to the scope of the invention. Accordingly, it is intended, by the appended claims, to cover all modifications of the invention which fall within the true spirit and scope of the invention.

We claim:

1. An integrated circuit, comprising:

an address bank decoder for decoding an address bank signal to provide a first one of a plurality of bank enable signals, the address bank decoder having an input for receiving the address bank signal and a plurality of outputs wherein each of the plurality of outputs provides a respective one of the plurality of bank enable signals;

an input data decoder for decoding an input data bank signal to provide a first one of a plurality of input enable signals, the input data decoder having an input for receiving the input data bank signal and a plurality of outputs wherein each of the plurality of outputs provides a respective one of the input enable signals;

an output data decoder for decoding an output data bank signal to provide a first one of a plurality of output enable signals, the output data decoder having an input for receiving the output data bank signal and a plurality of outputs wherein each of the plurality of outputs provides a respective one of the output enable signals; and

a plurality of memory banks wherein each of the plurality of memory banks is concurrently accessible, each of the plurality of memory banks, comprising:

a first latch for selectively storing a first address value in response to a first enable signal;

a second latch for selectively storing a first data value in response to a second enable signal;

a third latch for selectively storing a second data value in response to a third enable signal;

a fourth latch for selectively storing a first control value in response to a fourth enable signal;

logic means for selectively asserting the first enable signal, the second enable signal, the third enable signal, and the fourth enable signal when a corresponding one of the plurality of bank enable signals is in a predetermined logic state, the logic means being coupled to each of the first latch,

the second latch, the third latch, and the fourth latch; and

an array of memory storage elements for selectively communicating a digital information value, the array of memory storage elements being coupled to each of the first latch, the second latch, the third latch, and the fourth latch;

wherein a first one of the plurality of memory banks executes a first data communication operation subsequent to latching the first address value, the first control value, and one of the first and second data values and a second one of the plurality of memory banks executes a second data communication operation subsequent to latching a second address value, a second control value, and a third data value, the second one of the plurality of memory banks executing the second data communication operation concurrently with the first one of the plurality of memory banks executing the first data communication operation.

2. The integrated circuit of claim 1 wherein the first control signal indicates that the first one of the plurality of memory banks should perform one of a read and a write data operation and the second control signal indicates that the second one of the plurality of memory banks perform one of the read and the write data operation.

3. The integrated circuit of claim 1 wherein the first address value stored in the first latch of a first one of the plurality of memory banks corresponds to a first memory storage element in the array of memory storage elements.

4. The integrated circuit of claim 3 wherein when the first control signal is in a first logic state, the first memory storage element is enabled to perform a memory read operation and when the first control signal is in a second logic state, the first memory storage element to perform a memory write operation.

5. The integrated circuit of claim 1 wherein the logic means logically combines the corresponding one of the plurality of bank enable signals and an address strobe signal to provide the first latch signal.

6. The integrated circuit of claim 1 wherein the logic means logically combines a corresponding one of the plurality of data input bank enable signals and a data input strobe signal to provide the second latch signal.

7. The integrated circuit of claim 1 wherein the logic means logically combines a corresponding one of the plurality of data output bank enable signals and a data output strobe signal to provide the third latch signal.

8. The integrated circuit of claim 1 wherein the logic means logically combines the corresponding one of the plurality of bank enable signals and an address strobe signal to provide the fourth latch signal.

9. A method for accessing a memory in an integrated circuit, comprising the steps of:

receiving a first instruction for executing a first memory operation, the first instruction indicating a first memory location;

decoding the first instruction to indicate a first one of a plurality of memory banks to be accessed during execution of the first memory operation;

storing a first address value in a first latch circuit in the first one of the plurality of memory banks, the first address value corresponding to a first memory location in the first one of the plurality of memory banks;

storing a first control value in a second latch circuit in the first one of the plurality of memory banks, the first control value indicating a type of memory operation to be executed, the type of memory operation being one of a read memory operation and a write memory operation;

receiving a second instruction for executing a second memory operation, the second instruction indicating a second memory location to be accessed;

decoding the second instruction to indicate a second one of the plurality of memory banks to be accessed during execution of the second memory operation;

storing a second address value in a first latch circuit in the second one of the plurality of memory banks, the second address value corresponding to a second memory location in the second one of the plurality of memory banks;

storing a second control value in a second latch circuit in the second one of the plurality of memory banks, the second control information value indicating the type of memory operation to be executed; and

concurrently executing the first memory operation in the first one of the plurality of memory banks and the second memory operation in the second one of the plurality of memory banks.

10. The method of claim 9 further comprising the steps of:

storing a first data value in a third latch circuit of the first one of the plurality of memory banks;

enabling the third latch circuit to output the first data value to a driver circuit when the first control information indicates that the first memory operation is the write memory operation;

enabling the first latch circuit to output the first address value stored therein;

accessing the first memory location in the first one of the plurality of memory banks in response to the first address value; and

writing the first data value in the first memory location.

11. The method of claim 10 further comprising the steps of:

enabling the first latch circuit to output the first address value stored therein;

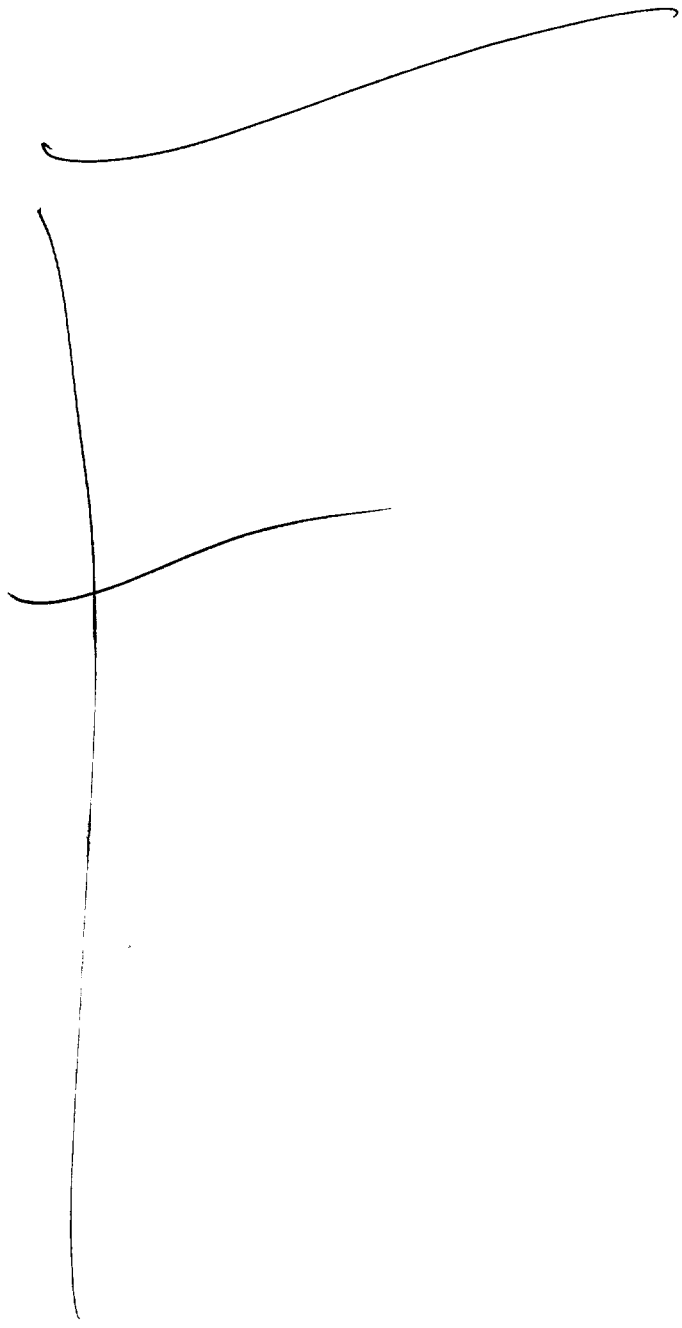
accessing a stored data value from the first memory location in the first one of the plurality of memory banks in response to the first address value;

storing the stored data value in a fourth latch circuit when the first control information indicates that the first memory operation is the read memory operation;

enabling the fourth latch circuit to providing the stored data value to an output driver circuit; and

enabling the output driver circuit to provide the stored data value in response to an external data output control value.

* * * * *



United States Patent [19]

Pelley, III

[11] **Patent Number: 4,794,434**

[45] **Date of Patent: Dec. 27, 1988**

[54] **TRENCH CELL FOR A DRAM**

[75] Inventor: **Perry H. Pelley, III,** Austin, Tex.

[73] Assignee: **Motorola, Inc.,** Schaumburg, Ill.

[21] Appl. No.: **69,916**

[22] Filed: **Jul. 6, 1987**

[51] **Int. Cl.**[4] **H01L 29/78;** H01L 29/06; H01L 27/02

[52] **U.S. Cl.** **357/23.6;** 357/55; 357/43

[58] **Field of Search** 357/23.6, 55, 43

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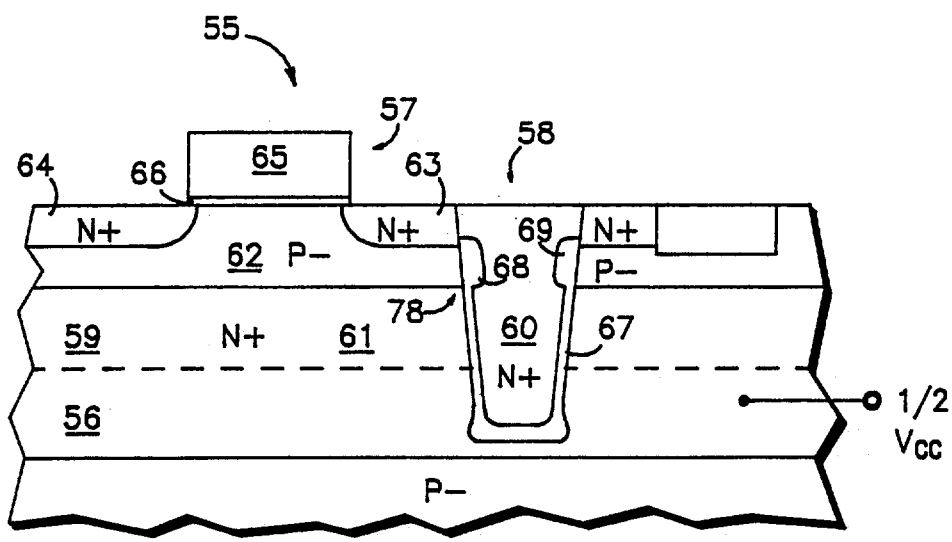
Primary Examiner—Martin H. Edlow
Assistant Examiner—Robert P. Limanek
Attorney, Agent, or Firm—John A. Fisher; Jeffrey Van Myers; James L. Clingan, Jr.

[57] **ABSTRACT**

A DRAM memory cell has a trench capacitor and a transistor. The trench of the trench capacitor penetrates to a buried layer which acts as the primary portion of one of the plates of the capacitor. When the buried layer is the same conductivity type as the transistor of the memory cell, the buried layer is biased to a voltage selected to reduce the maximum voltage across the capacitor. This allows for a reduction in the thickness of the dielectric which coats the trench which increases the capacitance of the capacitor. When the buried layer is of the opposite conductivity type from the transistor type of the memory cell, there is no parasitic MOS transistor formed between the primary portion of the capacitor plate and the source of the transistor of the memory cell.

15 Claims, 4 Drawing Sheets



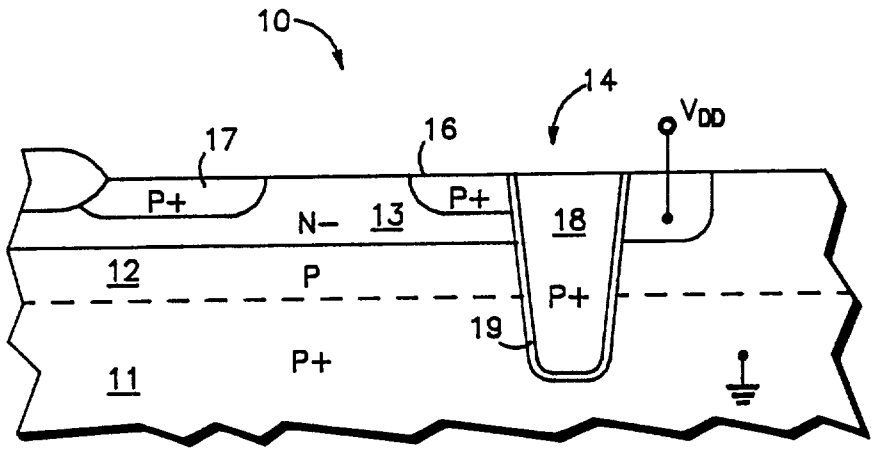


FIG. 1
—PRIOR ART—

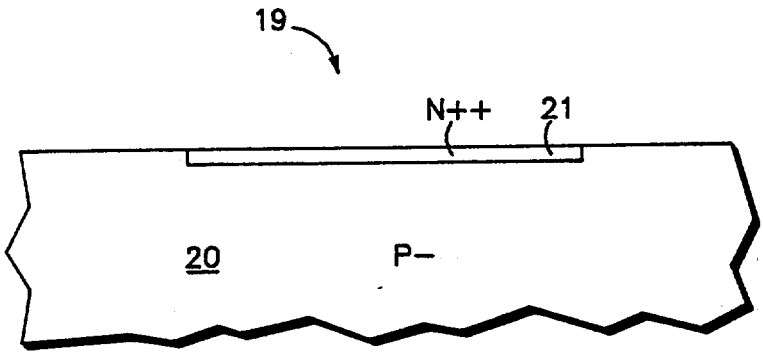


FIG. 2
—PRIOR ART—

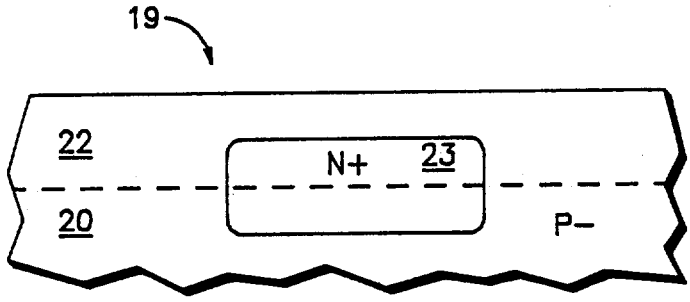


FIG. 3
−PRIOR ART−

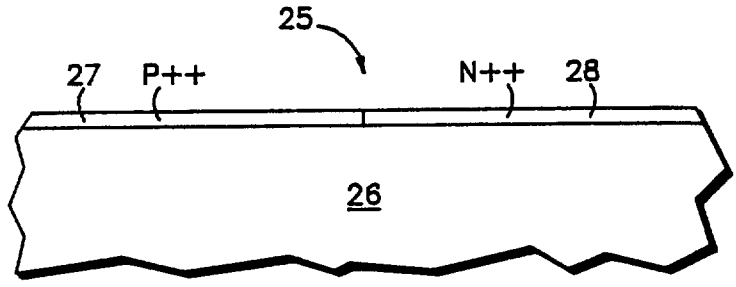


FIG. 4
−PRIOR ART−

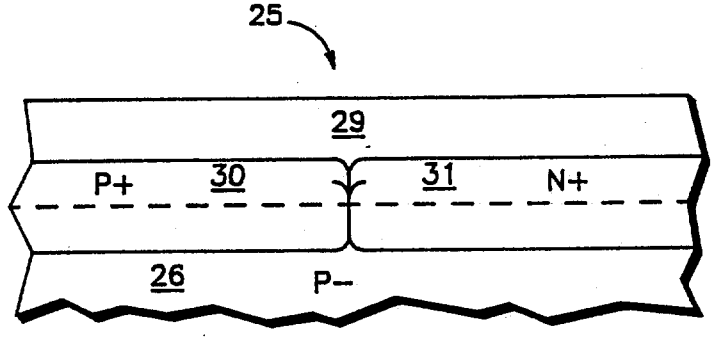
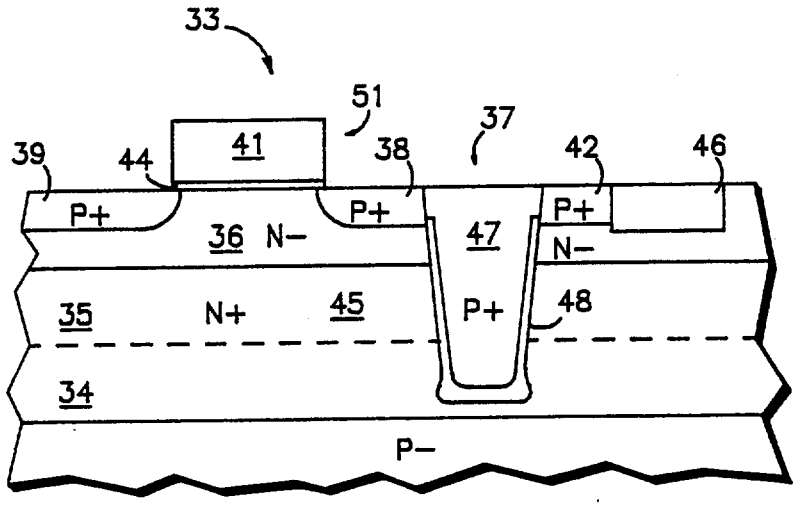


FIG. 5
−PRIOR ART−


33
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44
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P+
P+
P+
36 N−
47
N−
35
N+
45
P+
48
34
P−

FIG. 6

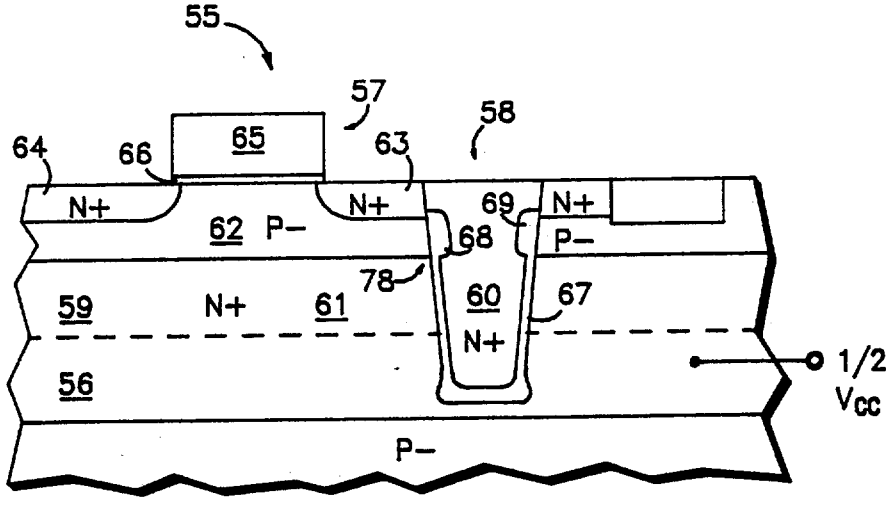

55
57
58
64
66
65
63
N+
N+
69
N+
62 P−
68
P−
78
59
N+
61
60
67
N+
56
1/2
Vcc
P−

FIG. 7

FIG. 8

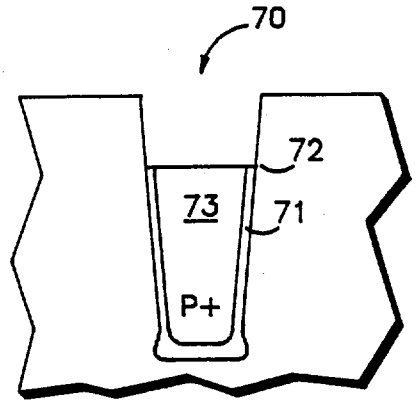


FIG. 9

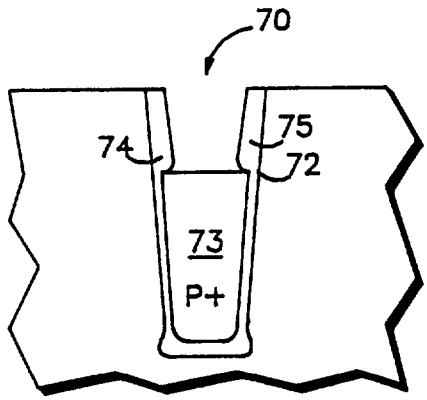
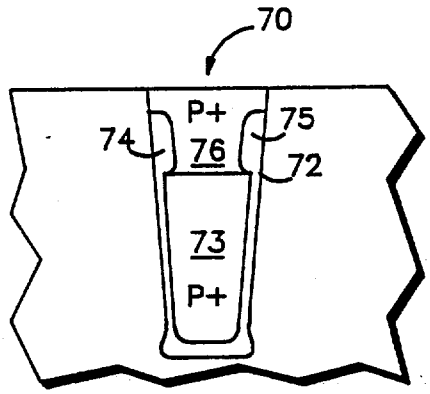


FIG. 10



TRENCH CELL FOR A DRAM

FIELD OF THE INVENTION

The present invention relates to dynamic random access memory (DRAM) cells, and more particularly, to DRAM cells which are formed using a trench.

BACKGROUND OF THE INVENTION

A DRAM cell, formed of a transistor and a capacitor, is widely known. It has further become known to use a trench formed in the substrate as the capacitor of the DRAM cell. The advantage of a trench DRAM cell is an increase in area of the plates of the capacitor for a given surface area of the substrate. In constructing an array or subarray of DRAM cells, trench or otherwise, it is common for each of the capacitors in the array or subarray to have a common plate which is in common with the other cells in the array or subarray and have an individual plate which is connected to the transistor of the cell. In a trench DRAM cell, the individual plate can be either inside the trench or outside the trench. If it is outside the trench, there is a difficulty in keeping the individual plates of adjoining cells from diffusing together. If the individual plate is on the inside, there are also problems most of which are common to either approach.

Even with the increased plate area of a trench capacitor, it is still desirable to have more capacitance in the cell capacitor. One way to increase capacitance is to increase the doping level of the area outside the trench. This has the potential disadvantage of adversely affecting the transistors formed in the substrate. The transistors have better performance characteristics if the doping level is lower than that which is optimum for increasing the capacitance of the capacitor. An example in the prior art of addressing this problem is shown in FIG. 1 which shows a portion of a trench cell 10 formed in a substrate 11 which includes an epitaxial layer 12. This approach uses a P channel array formed in an N well 13 with P channel starting material. Epitaxial layer 12 is grown over substrate 11 which began as highly doped P+ silicon. The resulting epitaxial layer 12 of silicon is a lesser doped P silicon which is used for the formation of N channel transistors in the circuits which are peripheral to the array. N well 13 is then formed in a portion of epitaxial layer 12 doped to only N− for improved transistor performance. Well 13 is coupled to a positive voltage, such as 5 volts, which is shown as VDD in FIG. 1. Substrate 11 is coupled to a negative supply terminal such as ground shown in FIG. 1. Well 13 can be pumped to a voltage higher than the positive power supply VDD and, similarly, substrate 11 can be pumped to a more negative voltage as desired for circuit performance. A trench capacitor 14 is formed through N well 13 and epitaxial layer 12 and into substrate 11. Formed in well 13 is a source 16 and a drain 17. Source 16 and drain 17 are the source and drain of the transistor which, along with capacitor 14 form DRAM cell 10. Capacitor 14 is filled with P+ polysilicon 18 which is dielectrically separated from substrate 11, epitaxial layer 12, and well 13 by an oxide layer 19. Alternatively, layer 19 could be an oxide-nitride-oxide sandwich instead of just oxide. In either case, layer 19 forms a dielectric for capacitor 14. One plate of capacitor 14 is polysilicon 18 which is connected to source 16. This connection to source 16 is not shown in FIG. 1 but is generally accomplished with a conductive strap but can also be accomplished by etching down layer 19 prior to filling the trench with polysilicon 18 so that polysilicon 18 is in direct contact with source 16. The other plate is a combination of substrate 11, epitaxial layer 12, and well 13. Most of the contribution to the capacitance of capacitor 14 is from the substrate because it has a much higher doping concentration than epitaxial layer 12. Well 13 will provide very little contribution because it is lightly doped for transistor performance reasons.

Even though well 13 is lightly doped, there is a limit to how lightly it can be doped because of a parasitic MOS transistor formed between epitaxial layer 12 and source 16. Well 13 acts as the channel, polysilicon 18 acts as the gate, and layer 19 acts as the insulator between the gate and channel. Even a leakage current as low as 1 picoamp will remove the charge stored in capacitor 14 before it can be read and refresned. If well 13 is too lightly doped, the threshold voltage of this parasitic transistor is sufficiently low that it will be at least partially conductive and leak at the 1 picoamp rate which ensures loss of data. This lower concentration is desirable because the regular MOS transistors in well have their threshold adjusted by an implant. If the doping level in well 13 is high enough to ensure that the parasitic transistor will not leak off charge from capacitor 14, the threshold adjust implant will not be optimum. The threshold adjust implant is advantageous because, for a given threshold voltage, the body effect is less on a transistor which has had its threshold increased to that give threshold voltage by an implant than on a transistor whose threshold voltage is at the given threshold voltage by virtue of the doping concentration of the well or substrate in which it is formed. The optimum concentration of well 13 is sufficiently low that there would be leakage through the parasitic transistor of sufficient magnitude to destroy cell data, especially when doping variations due to manufacturing variations are taken into account. Process variations during the fabrication of the integrated circuit will result in even lower doping concentrations for some devices. This is handled by raising the target concentration which will thus raise the nominal doping concentration even further beyond the optimum concentration for well 13.

SUMMARY OF THE INVENTION

An object of the present invention is to provide an improved DRAM.

Another object of the present invention is to provide an improved DRAM memory cell.

Yet another object of the invention is to provide improved trench DRAM memory cell.

These and other objects are achieved in a semiconductor body including a substrate doped to a first concentration and a buried layer of a second concentration greater than said first concentration formed below a surface of said substrate. The semiconductor body has a memory cell comprises a transistor and a trench capacitor. The transistor has a gate and a conduction path. The trench capacitor is coupled to one side of the conduction path and is formed of a trench which penetrates the surface and into said buried layer.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross-section of a portion of a trench DRAM cell device according to the prior art; and

FIG. 2 is a cross-section of a substrate at an early stage in processing according to the prior art;

FIG. 3 is a cross-section of the substrate in FIG. 2 at a later stage in processing showing a buried layer according to the prior art;

FIG. 4 is a cross-section of a substrate at an early stage in processing according to the prior art;

FIG. 5 is a cross-section of the substrate in FIG. 4 at a later stage in processing showing two buried layers according to the prior art;

FIG. 6 is a cross-section of a DRAM well according to a first embodiment of the invention;

FIG. 7 is a cross-section of a DRAM cell according to a second embodiment of the inventinn;

FIG. 8 is a cross-section of a trench used in the DRAM cell of FIG. 7 at a stage in processing;

FIG. 9 is a cross-section of the trench of FIG. 8 at a subsequent stage in processing; and

FIG. 10 is a cross-section of the trench of FIG. 9 at a subsequent stage in processing.

DESCRIPTION OF THE INVENTION

As shown in FIG. 1, the use of an epitaxial layer for manufacturing a DRAM is in the prior art. Another feature available in prior art processing is a buried layer. The invention uses a buried layer as an important part of a trench DRAM cell. Shown in FIG. 2 is portion 19 of an integrated circuit having a P− substrate 20 and an N++ region 21 formed in the surface of substrate 20. Shown in FIG. 3 is substrate 20 after an epitaxial layer 22 has been grown. A dotted line is shown between substrate 20 and epitaxial layer 22. After processing the integrated circuit, doped portion 21 in FIG. 2 expands to an N+ buried layer 23 which is in both substrate 20 and epitaxial layer 22. Epitaxial layer 22 is P-type but can be any desired concentration for optimum circuit performance. A buried layer such as buried layer 23 is commonly found in integrated circuits which have bipolar transistors including integrated circuits which have both bipolar transistors and MOS transistors. The buried layer is for collectors of bipolar transistors. Such integrated circuits which have both bipolar and MOS transistors are often referred to as being "BiMOS." BiMOS appears to be increasing in popularity for integrated circuits, particularly memories, including Drams.

Shown in FIG. 4 is a cross-section of a portion of an integrated circuit 25 having a substrate 16, a P++ region 28, and an N++ region 28 at a stage in a BiMOS process for forming a pair of adjoining buried layers. Shown in FIG. 5 is the portion of integrated circuit 25 of FIG. 4 after growing an epitaxial layer 29 and after other processing. This results in the formation of a P+ buried layer 30 and an N+ buried layer. Because regions 27 and 28 of FIG. 1 are adjoining, the resulting buried layers 30 and 31 are also adjoining. The location of regions 27 and 28 determine the location of buried layers 30 and 31. Thus a buried layer can be either the same or the opposite conductivity type as the substrate. Buried layers are typically biased to some desired voltage. Buried layers of the same conductivity type as the substrate are, of course, biased to the same voltage as the substrate. Buried layers of the opposite conductivity of the substrate can be electrically isolated from the substrate if the PN junction between the buried layer and the substrate is not forward biased.

Shown in FIG. 6 is a cross-section of a memory cell 33 comprised of a substrate 34, an epitaxial layer 35, an N− well 36, a trench capacitor 37, a P+ source 38, a P+ drain 39, a gate 41, a P+ contact 42, an oxide isolation region 46, a gate insulator 44, and a N+ buried layer 45. Substrate 34 and epitaxial layer 35 are known as separated by a dotted line. Source 38, drain 39 and a portion of well 36 therebetween forms a conventional conduction path controlled by gate 41. This conduction path, which is on one side of capacitor 37, is connected to capacitor 37 via source 38. Buried layer 45 is in both the epitaxial layer 35 and substrate 34. Trench capacitor 37 is formed from a trench etched into the semiconductor body comprised of epitaxial layer 35 and substrate 34. Trench capacitor 37 is filled with a P+ polysilicon 47. Polysilicon 47 is dielectrically insulated from buried layer 45 and well 36 by an insulating layer shown as dielectric 48. A bottom portion of dielectric 48 is intentionally enlarged. This is achieved by an oxygen implant. The oxygen reacts with the silicon of substrate 34 to form an enlarged area of oxide. It has been found, in the prior art, that this bottom area of the trench is more vulnerable to punchthrough so that the increased thickness in this area is desirable. Polysilicon 47 is in contact with source 38 by virtue of dielectric 48 having been etched down. This etching down of the dielectric of the trench capacitor is known. A P channel transistor 51 is formed of source 38, drain 39, and gate 41. Transistor 51 and capacitor 37 form memory cell 33. Region 42 is formed during the formation of source 38 and is present for alignment tolerance. Polysilicon 47 is one plate on capacitor 37. Buried layer 55 has a portion adjacent to dielectric 48. Well 36 also has a portion adjacent to dielectric 48. These portions of well 36 and buried layer 45 which are adjacent to dielectric 48 form a second plate of capacitor 37. The primary contribution to the capacitance of capacitor 37 is from buried layer 45 which is of a high concentration of N-type dopant. Thus, except for the contribution from well 36, the capacitance of capacitor 37 is all from a high doping concentration. This advantage of increasing the capacitance with a high doping concentration does not cause a decline in performance of transistors because the buried layer, as its name suggests, does not reach the surface. By having N well 36 extend down to buried layer 445, there is no parasitic MOS transistor between source 38 and the region which contributes to the capacitance of capacitor 37. The portion of substrate 34 which is P− is separated from source 38 by buried layer 45. There is thus no danger of fomming even a marginally conductive MOS transistor between substrate 34 and source 38. Memory cell 33 thus offers an advantage over that shown in FIG. 1. Additionally, in the case in which the DRAM is to be BiMOS, there is no increased process complexity because buried laeers are part of the typical BiMOS process.

Shown in FIG. 7 is a memory cell 55 formed with a P−substrate as starting material and comprised generally of a transistor 57 and a trench capacitor 5. An epitaxial layer 59 is grown on substrate 56. Substrate 56 is below the dotted line and epitaxial layer 59 is above the dotted line. An N+ buried layer is formed in both epitaxial layer 59 and substrate 56. Trench capacitor 58 is filled with N+ polysilicon 60 to form a first plate of capacitor 58. Transistor 57 is formed in a P− well 62. Well 62, although of the same conductivity type as the P− portion of substrate 34, is separately doped. Both the P channel transistors and the N channel transistors are formed nn wells. This is known as a twin well process which is typical for MOS integrated circuits which

have an epitaxial layer. The wells which are of the same conductivity type astthe starting material of the substrate are at the same voltage. In the present case the starting material of the substrate, substrate **56**, is P-type conductivity so that the P wells will be biased to the same potential as substrate **56**. Well **62** will then be biased to the same voltage as the P− portion of substrate **56**, which may be, for example, ground potential. Transistor **57** includes a source region **63**, a drain region **64**, and a polysilicon gate **65**. A gate insulator **66** insulates gate **65** from well **62**. Trench capacitor **58** includes a dielectric **67** is the dielectric for capacitor **58**. Buried layer **61** has a portion which adjoins dielectric **67**. Well **62** also has a portion which adjoins dielectric **67**. The portions of well **62** and buried layer **61** form a second plate of capacitor **58**. Dielectric **67** includes a thicker portion **68** and a thicker portion **69**. As shown in FIG. **7**, trench capacitor **58** is formed from a trench etched into a semiconductor body in which one plate is the semiconductor body adjacent to the trench and the other plate is conductive material which fills the trench. These two plates are separated by an insulating layer which lines the trench.

Dielectric **67** is formed as a thin laver which may be, for example, **170** Angstroms. Dielectric is then etched down from the surface. Subsequent thicker dielectric is then formed between the etched back portion and the surface. The thicker portion is then etched back to allow contact between polysilicon. These steps to form thicker portions **68** and **69** are depicted in more detail in FIGS. **8–10**. Shown in FIG. **8** is a trench **70** with a dielectric **71** coating the surface thereof but etched down to a line **72** to which trench **70** is filled with P+ polysilicon **73**. Shown in FIG. **9** is trench **70** with additional thicker dielectric portions **74** and **75**. Shown in FIG. **10** is trench **70** with dielectric portions **74** and **75** etched back and P+ polysilicon **76** fills the remainder of trench **70** from line **72** to the surface. Portions **68** and **69** in FIG. **7** are analogous to portions **74** and **75** of FIG. **10**. P+ polysilicon **60** of FIG. **7** is analogous to polysilicon **73** and polysilicon **76** combined.

One reason for thicker portions **68** and **69** is to increase the threshold voltage of a parasitic MOS transistor **78**. The portion of well **62** between source **63** and buried layer **61** acts as a channel for parasitic transistor **78**. Buried layer **61** and source **63** act as source and drain and polysilicon **60** acts as a gate of transistor **78**. Portion **68** of dielectric **67** acts as the insulator between the gate and the channel of parasitic transistor **78**. The thickness of portion **68** and the doping of well **62** combine to ensure that parasitic transistor **62** is not conductive. Another reason for thicker portions **68** and **69** is to ensure there is no dielectric breakdown or punchtrough between well **62** and polysilicon **60** inside the trench. There will be times when the full power supply voltage differential will be applied between well **62** and polysilicon **60**. The reason for having the trench penetrate a buried layer which is biased to only ½ Vcc is to be able to reduce the dielectric thickness and thus increase capacitance.

Memory cell **55** has nn advantage over that of FIG. **1** because buried layer **61** can be electrically isolated from the P− portion of substrate **56** as well as other N wells. Buried layer **61** can thus be biased to a voltage which is, for examle, one half of the power supply voltage. This is shown as ½ Vcc in FIG. **7**. This reduces the maximum voltage which will be developed across dielectric **67**. With the reduction in maximum voltage, d;electric **67** can be made thinner which increases the capacitance of capacitor **58**. Memory cell **55** of FIG. **7** then is an improvement over that of FIG. **1** at least by providing increased capacitance by being able to reduce the dielectric thickness of the trench capacitor. Memory cell **33** of FIG. **6** is thus an improvement over that of FIG. **1** at least because it eliminates the parasitie MOS transistor. These advantages are a direct result of having the primary part of one of the plates of the trench capacitor of a DRAM cell be a buried layer. This is achieved by having the trench of the trench capacitor penetrate a buried layer.

In both embodiments, FIG. **6** and FIG. **7**, the trench of the trench capacitor penetrates a buried layer. The buried layer, as used herein, is a region in a semiconductor body which is below the surface of the semiconductor body and which is greater in concentration than the doping concentration of the starting material. As shown as being available from prior art processing, the buried layer may be either the same type of conductivity or opposite type conductivity of the starting material The method shown uses epitaxial growth to develop a buried layer This approach to forming a buried layer has been commonly done in forming bipolar transistors in integrated circuits. This approach has also been used in BiMOS processes. Another approach to forming a buried layer is to implant through the surface of the semiconductor body with sufficient energy so that the resulting doped region is sufficiently below the surface for the memory cell purpose. This approach may prove to be better. One reason it may prove to be better is that it may result in not needing to grow the epitaxial layer. In any event, the present invention is directed to a memory cell which has a trench capacitor which penetrates a buried layer not to how a buried layer is formed.

I claim:

1. In a semiconductor body including a substrate of a first conductivity and doped to a first concentration, an epitaxial layer grown on the substrate to form a surface of the semiconductor body, and a buried layer of a second conductivity and of a second concentration greater than said first concentration formed below said surface in a region overlapping the substrate and the epitaxial layer, a memory cell comprising:

a transistor having a gate and a conduction path; and

a trench capacitor coupled to one side of the conduction path, said trench capacitor formed of a trench which penetrates the surface and said buried layer, said trench capacitor characterized as having a first plate formed of conductive material inside the trench coupled to the conduction path, and a second plate, said second plate being substantially a portion of the buried layer adjacent to the trench.

2. In the semiconductor body of claim **1** wherein the memory receives a power supply voltage provided externally from the memory, the capacitor further characterized as having its second plate biased to a voltage which is between 30% and 70% of the power supply voltage.

3. In the semiconductor body of claim **2** wherein a well of the first conductivity type is formed in the epitaxial layer between the surface and the buried layer, the transistor further characterized as having a source, a drain, and a channel formed in the well and the well further characterized as having a portion adjacent to a portion of the trench above the buried layer.

4. In the semiconductor body of claim **3**, the capacitor further characterized as having an insulating layer

between the first plate and the portions of the well and the buried layer which are adjacent to the trench.

5. In the semiconductor body of claim 4, the insulating layer further characterized as having a first thickness along portions between the buried layer and the trench and a second thickness between the well and the trench, said second thickness being greater than said first thickness.

6. In the semiconductor body of claim 1 wherein a well of the first conductivity type is formed in the epitaxial layer between the suraace and the buried layer, the transistor further characterized as having a source, a drain, and a channel formed in the well and the well further characterized as having a portion adjacent to a portion of the trench above the buried layer.

7. In the semiconductor body of claim 6, the capacitor further characterized as having an insulating layer between the first plate and the portions of the well and the buried layer which are adjacent to the trench.

8. In a semiconductor body including a substrate, an epitaxial layer grown on the substrate to form a surface of the semiconductor body, and a well of a of a first conductivity type formed in said epitaxial layer, said epitaxial layer and said substrate having at least a region of a second conductivity type, a memory cell comprising;

a transistor having a gate and a conduction path formed in said well; and

a trench capacitor coupled to one side of the conduction path, said capacitor formed of a trench which penetrates the well and said region of the second conductivity type; said capacitor having a first plate formed of conductive material inside the trench coupled to the conduction path, and a second plate being substantially a portion of said region adjacent to the trench; and said capacitor having an insulating layer between the first plate and the well and between the first plate and said region, said insulating layer having a first thickness along portions between said region and the first plate and a second thickness between the well and the first plate, said second thickness being greater than said first thickness.

9. In a semiconductor body including a substrate of a first conductivity and doped to a first concentration and a buried layer of a second conductivity and of a second concentration greater than said first concentration formed below a surface of said substrate, a memory cell comprising;

a transistor having a gate and a conduction path; and

a trench capacitor coupled to one side of the conduction path, said trench capacitor formed of a trench which penetrates the surface and said buried layer, said trench capacitor characterized as having a first plate formed of conductive material inside the trench coupled to the conduction path, and a second plate, said second plate being substantially a portion of the buried layer adjacent to the trench.

10. In the semiconductor body of claim 9 wherein the memory receives a power supply voltage provided externally from the memory, the capacitor further characterized as having its second plate biased to a voltage which is between 30% and 70% of the power supply voltage.

11. In the semiconductor body of claim 10 wherein a well of the first conductivity type is formed in the surface of the substrate above the buried layer, the transistor further characterized as having a source, a drain, and a channel formed in the well and the well further characterized as having a portion adjacent to a portion of the trench above the buried layer.

12. In the semiconductor body of claim 11, the capacitor further characterized as having an insulating layer between the first plate and the portions of the well and the buried layer which are adjacent to the trench.

13. In the semiconductor body of claim 12, the insulating layer further characterized as having a first thickness along portions betwee the buried layer and the trench and a second thickness between the well and the trench, said second thickness being greater than said first thickness.

14. In the semiconductor body of claim 9 wherein a well of the first conductivity type is formed in the surface of the substrate above the buried layer, the transistor further characterized as having a source, a drain, and a channel formed in the well and the well further characterized as having a portion adjacent to a portion of the trench above the buried layer.

15. In the semiconductor body of claim 14, the capacitor further characterized as having an insulating layer between the first plate and the portions of the well and the buried layer which ar adjacent to the trench.

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United States Patent [19]

Remedi et al.

[11] **Patent Number: 4,511,914**

[45] **Date of Patent: Apr. 16, 1985**

[54] **POWER BUS ROUTING FOR PROVIDING NOISE ISOLATION IN GATE ARRAYS**

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[21] Appl. No.: **394,239**

[22] Filed: **Jul. 1, 1982**

[51] **Int. Cl.**[3] **H01L 27/02**; H01L 27/10; H01L 23/48; H01L 27/15

[52] **U.S. Cl.** **357/45**; 357/41; 357/68

[58] **Field of Search** 357/68, 45, 41

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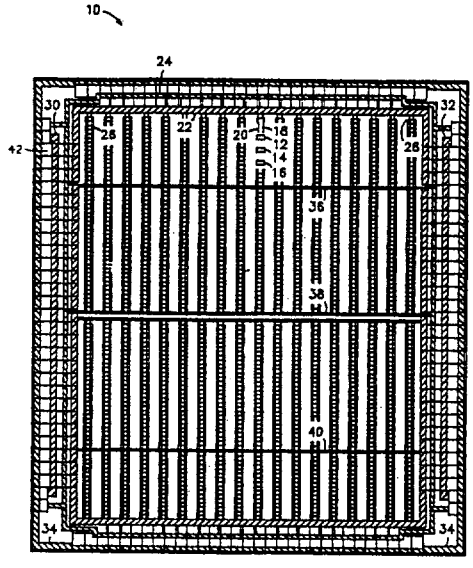
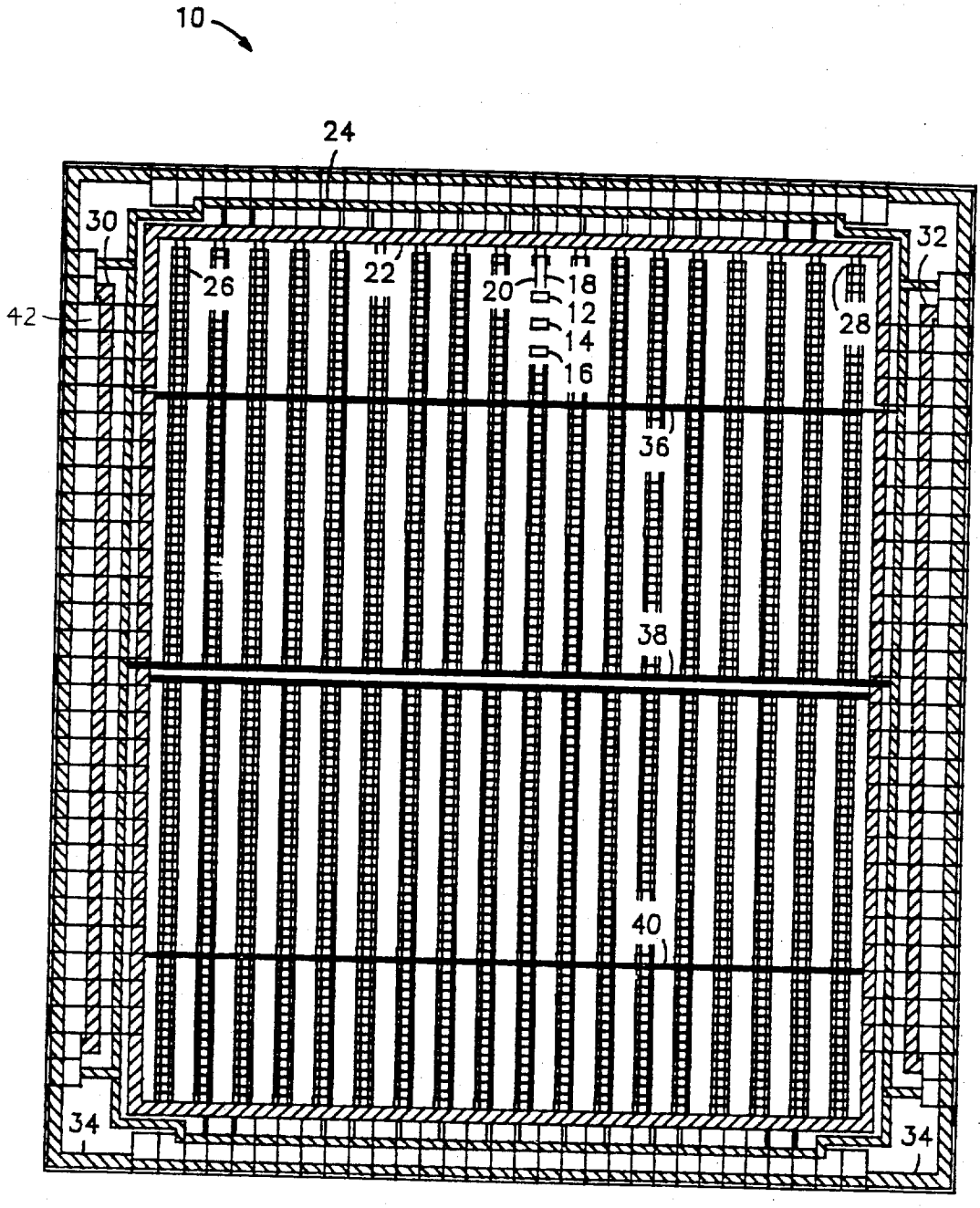
[57] **ABSTRACT**

A gate array which has power bus routing for increasing current availability to a plurality of transistor cells is provided. The gate array also has separate power busses for input/internal logic and output circuits. The gate array comprises n columns of transistor cells with two power busses extending substantially along each column to power the cells. Input/internal logic power busses and separate output power busses extend around the perimeter of the columns of transistor cells. At least one power strip for increasing current availability to the transistor cells is routed across the transistor cells substantially perpendicular to the n columns and is connected to both the power busses of each column and to the input/internal logic power busses.

9 Claims, 1 Drawing Figure

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POWER BUS ROUTING FOR PROVIDING NOISE ISOLATION IN GATE ARRAYS

TECHNICAL FIELD

This invention relates generally to gate arrays, and, more particularly, to power bus routing for gate arrays.

BACKGROUND ART

Gate arrays are uniform patterns of hundreds or thousands of unconnected transistor-level gate cells. Due to the availability to a designer of means to connect the cells via interlevel contacts and interlevel routing performed at a late stage in processing, many custom circuits may be created from a basic gate array. A basic design objective of gate arrays is to make the gate cells easily accessible to power and ground busses since the gate cells are typically placed on a level different from the power and ground busses. However, when hundreds or thousands of transistors are connected in an array, very large current spikes may develop in certain locations of the array when the transistors switch at the same time. When power busses are not routed closely to the transistors, noise may exist on internal nodes and create logic errors in the gate array cells. When current spikes exist at the inputs of the gate array, these spikes may also create logic errors in the internal portion of the gate array. Some gate arrays utilize separate digital and analog power and ground distribution busses to minimize analog circuit noise from digital circuitry as noted on page 166 of "CMOS Uncommitted Logic Arrays Are Part-Digital, Part-Analog", by Yoder, *Electronics*, Jan. 13, 1981. However, when such gate arrays have a large plurality of input/output cells per side of the array, large current spikes at the output may still generate noise errors in the internal digital circuitry.

BRIEF SUMMARY OF THE INVENTION

It is an object of the present invention to provide a gate array having improved power bus routing.

Another object of the present invention is to increase current availability to transistor cells in a gate array without substantially modifying existing power bus routing.

Another object of the present invention is to provide an improved gate array which reduces noise present in internal circuitry and which reduces the presence of current spikes from transistor switching.

Yet another object of the present invention is to provide an improved gate array which isolates noise at the input/output cells from the internal circuitry.

In carrying out the above and other objects and advantages of the present invention, there is provided, in one form, a gate array having n parallel columns of a plurality of transistor cells, where n is an integer. Each column, in the preferred form, has first and second power busses which extend from end to end of the column and which provide power to the transistor cells. The first and second power busses are coupled to first and second voltage potential lines. A pair of output power busses are positioned parallel to an outer side of both a first and an nth column of the n columns. Each pair of output power busses is substantially parallel to said n columns and coupled to the first and second voltage potential lines. Separate power busses in the form of first and second input/internal logic power busses extend substantially around the perimeter of said n columns and between the n columns and the output power busses. Additionally, at least one power strip extends substantially perpendicular to said n columns to connect input/internal power busses with the first and second power busses of each column to provide increased current availability to the transistor cells. The above and other objects, features and advantages of the present invention will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawing.

BRIEF DESCRIPTION OF THE DRAWING

The single FIGURE illustrates in graphic form a gate array constructed in accordance with a preferred embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Shown in the single drawing is a gate array **10** having n columns of transistor cells, such as column **12** having cells **14** and **16**, where n is an integer. Although in a preferred form eighteen columns of transistor cells are shown, any number of columns and cells may be used to practise the invention. If gate array **10** is viewed from the left or right side of the drawing, the columns can be considered as rows. Extending the entire length of each of the n columns are first and second power busses, such as power bus **18** and power bus **20** in column **12**. The first and second busses in the n columns are coupled to a first and a second voltage potential line, respectively, by coupling each power bus to either an input/internal logic power bus **22** or an input/internal logic power bus **24**. It should be noted that not all gate arrays have a plurality of continuous columns of transistor cells, but rather may have columns of cells divided into two or more sections. For gate arrays having sectioned columns of transistor cells, power busses, such as power busses **18** and **20** may not extend the entire length of each column across the plural sections. However, this invention may be practised for gate arrays having any variety of structural organization of transistor cells. In a preferred form, input/internal logic power bus **22** is at a V_{SS} potential and extends substantially around the perimeter of the n columns. Input/internal logic power bus **24** is at a V_{DD} potential and also extends substantially around the perimeter of the n columns in a preferred form. Conventionally, the V_{DD} potential is a positive voltage potential and the V_{SS} potential is more negative than V_{DD} although V_{DD} is not necessarily a positive voltage potential. Although input/internal logic power busses **22** and **24** encircle the n columns for noise reduction purposes, the input/internal logic power busses need only to be long enough to be physically connected to each pair of power busses of the n columns. On the outer sides of a first column **26** and an nth column **28** are output power busses **30** and **32**, respectively, which are coupled to voltage potential V_{DD}. Extending around the outside perimeter of gate array **10** is an output power bus **34** which is coupled to V_{SS} potential. The output power busses are so designated because they primarily supply power to output circuits. Output power busses **30** and **34** form a first pair of output busses which, in a preferred form, extend substantially parallel to and along the outside edge of first column **26**. Similarly, output power busses **32** and **34** form a second pair of output busses which extend substantially parallel to and along the outside edge of nth column **28** in a preferred form. In yet another form of

the invention, output power busses 30 and 32 may be extended in part, or substantially around the perimeter of the n columns. Further, output power busses 30 and 32 may extend substantially parallel to output power bus 34 and be connected to function as a single output power bus. Power strips 36, 38 and 40 extend substantially perpendicular to the n columns and are coupled to busses 22 and 24 at each end at the outside edge of columns 26 and 28. Power strips 36, 38 and 40 each comprise first and second conductive busses, the first of which is connected to input/internal logic power bus 22 at the outside edge of columns 26 and 28. The second conductive bus of power strips 36, 38 and 40 is connected to input/internal logic power bus 24 at the outside edge of columns 26 and 28. In the preferred form, the power busses in the n columns, such as power busses 18 and 20, are routed on a first layer of metal which is covered by an insulating dielectric layer. Power strips 36, 38 and 40 are routed on a second layer of metal so that power strips 36, 38 and 40 do not electrically short circuit the transistor cells of the n columns. The conductive busses of strips 36, 38 and 40 which are connected to input/internal logic power bus 22 are also connected to the first power bus of each column, such as power bus 18 in column 12. This connection is made by cutting a hole, or a via, through the dielectric separating the n columns from power strips 36, 38 and 40. The conductive busses of strips 36, 38 and 40 which are connected to internal logic power bus 24 are connected to the second power bus of each column, such as power bus 20 in column 12. In the preferred form, three power strips are utilized and the first and second conductive busses of power strip 38 are made twice as large as the conductive busses of power strips 36 and 40. However, the invention may be practised with one or any plurality of power strips. It should also be noted that power strips 36, 38 and 40 need not necessarily extend across all the columns of gate array 10. Current availability may be increased by using some or all power strips across only a portion of the n columns.

In operation, a gate array, regardless of what type of process is used to manufacture the array, will usually develop very large current spikes when the transistors in the transistor cells switch. An entire column of transistors may switch at the same time and generate current in the hundreds of milliamperes range. Such current spikes can change the internal logic circuitry and create erroneous data. Conventional power bus routing is not sufficient to keep voltage drops in the cells associated with the current spikes from becoming excessive. Furthermore, in gate arrays there are typically a large number of output cells such as output cell 42 on one or more sides of the gate array with each cell having a contact pad. With a large number of output cells existing, the possibility for large AC and DC loads to be applied thereto exists. Therefore to keep current spikes from entering the array matrix, power busses, such as busses 30, 32 and 34, which are separate from the power busses of the internal logic circuitry and input pads, such as busses 22 and 24, may be used for the output circuits.

To substantially reduce the size of current spikes in each column, the effective ohmic length of the power busses of the n columns is reduced by adding power strips 36, 38 and 40 and connecting them to the power busses of the n columns. If power strips 36, 38 and 40 are routed on a different layer of metal and separated from the power busses of the n columns by a dielectric layer, the logic routing of a conventional gate array has not been disrupted. By now it should be appreciated that a gate array having power routing which separates current spikes in the output cells from internal digital logic and input pins and which minimizes current spikes in the digital logic has been provided.

By having input/internal logic power busses which are separate from output power busses, noise external to gate array 10 is effectively isolated. Furthermore, when separate power busses are used in this manner, the busses may be coupled to different leads in an integrated circuit package and different voltage levels applied thereto.

While the invention has been described in the context of a preferred embodiment, it will be apparent to those skilled in the art that the present invention may be modified in numerous ways and may assume many embodiments other than that specifically set out and described above. Accordingly, it is intended by the appended claims to cover all modifications of the invention which fall within the true spirit and scope of the invention.

We claim:

1. A gate array having power bus routing for providing noise isolation, comprising:

n columns of a plurality of transistor cells, where n is an integer, each of said n columns of transistor cells having first and second power busses extending substantially along each of the n columns and coupled to predetermined ones of the transistor cells;

first and second input/internal power busses coupled to said first and second power busses of each column, respectively, and extending substantially around the perimeter of said n columns, for providing power to each transistor cell of said n columns;

at least one power strip extending substantially perpendicular to said n columns of transistor cells, coupling each of said pair of input/internal power busses to a predetermined one of said first and second power busses of one or more columns, for providing increased current to said plurality of transistor cells; and

output power busses positioned along the outer perimeter of said gate array, for providing power busses for output cells along one or more sides of the gate array which are separate from the internal power busses to keep external current spikes from being coupled into the array.

2. The gate array of claim 1 wherein said output power busses further comprise:

a first output power bus positioned completely around the perimeter of the gate array; and

second and third output power busses positioned parallel to and between the first output power bus and said first and nth columns, respectively, wherein the first output power bus provides a first voltage potential and said second and third output power busses each provide a second voltage potential.

3. The gate array of claim 1 wherein said first and second power busses of each of said n columns are routed on a first conductive layer and said at least one power strip is routed on a second conductive layer which is separated from said first conductive layer by a dielectric layer.

4. The gate array of claim 1 wherein said at least one power strip comprises three power strips extending substantially perpendicular to said n columns and

spaced apart to divide said gate array into four sections of substantially equal area.

5. A gate array having n columns of a plurality of transistor cells, where n is an integer, and a plurality of output cells along one or more sides of the gate array, each of said n columns of transistor cells having first and second power busses coupled to first and second voltage potential lines, respectively, and extending substantially along each of the columns, comprising:

a power strip extending substantially perpendicular to said n columns, and coupling said first and second power busses to said first and second voltage potential lines, respectively, for providing increased current capability to said plurality of transistor cells; and

output power busses positioned along an outer perimeter of the gate array, for providing power busses for the output cells which are separate from the first and second voltage potential lines used to provide power to the transistor cells, said output power busses keeping external current spikes from being coupled into the array.

6. The gate array of claim 5 further comprising three power strips extending substantially perpendicular to said n columns from the first to the nth column and spaced a substantially equal distance apart, said second power strip located between said first and third power strips, wherein the width of said second power strip is substantially larger than the width of said first and third power strips.

7. A gate array having improved noise isolation, comprising:

n columns of a plurality of transistor cells, where n is an integer, each of said n columns of transistor cells having first and second power busses extending substantially along the columns and coupled to first and second voltage potential lines, respectively;

a plurality of output cells along one or more sides of the gate array, for interfacing between the transistor cells and external circuitry;

a pair of output power busses positioned on each side of said n columns and extending substantially parallel to said n columns, each pair of output power busses providing power only to the output cells; and

first and second input/internal power busses coupled to said first and second voltage potentials, respectively, and extending substantially around the perimeter of said n columns and extending between said n columns and said output power busses, for providing power only to the n columns of transistor cells.

8. The gate array of claim 7 wherein one output power bus of both pairs of output power busses which are positioned on each side of said n columns further extends substantially around the perimeter of said n columns.

9. A method of isolating noise from an external source in a gate array having a plurality of transistor cells arranged in n columns, where n is an integer, and having a plurality of output cells along one or more sides of the gate array, each column having first and second power busses extending substantially along each of said columns, comprising the steps of:

providing a plurality of internal power strips along both ends of said n columns and electrically coupled to the first and second power busses of said n columns, to provide power for only the n columns of transistor cells; and

providing a plurality of output power strips along the perimeter of the gate array, to provide power for only the output cells.

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